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A New Quadratic High Step-Up DC–DC Converter with Single Two-Winding Coupled-Inductor for Photovoltaic Systems Application

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Abstract: This article introduces a new quadratic high step-up DC–DC converter designed for renewable energy applications. The proposed converter combines a conventional boost topology with a two-winding coupled inductor (CI) to obtain a high voltage conversion ratio. The voltage gain is determined by both the duty ratio and the coupled-inductor turns ratio; however, the duty ratio serves as the primary control variable, whereas the turns ratio is selected as a design parameter according to the required voltage-conversion ratio. The proposed topology provides several important advantages, including high voltage gain, reduced voltage stress on the power switch, and a common ground between the input and output terminals, which simplifies system integration. A comparative evaluation with existing high-gain converter topologies confirms the improved voltage conversion performance and overall operating characteristics of the proposed design. The performance of the proposed converter is evaluated through analytical analysis and PSCAD/EMTDC based simulations at a switching frequency of 50 kHz, boosting an input voltage of 20 V to a regulated output voltage of 280 V.

Keywords: quadratic high step-up DC–DC converter; single switch; photovoltaic systems; coupled inductor; common ground

1. Introduction

The extensive utilization of fossil fuels has led to growing environmental concerns, primarily due to greenhouse gas emissions and their contribution to global warming. In addition, the limited availability of these conventional energy resources poses a significant challenge to satisfying the continuously increasing worldwide electricity demand. Consequently, renewable energy technologies, particularly solar and wind energy, have attracted considerable interest as sustainable alternatives. Among these resources, photovoltaic (PV) systems have become one of the most promising solutions because of their abundant energy source, long operational lifetime, and capability to generate electricity without producing harmful emissions [1,2]. Despite these advantages, the relatively low output voltage of PV modules, typically in the range of 10–50 V, prevents their direct connection to conventional power systems that require much higher voltage levels. Therefore, DC–DC converters play a crucial role in renewable energy systems by stepping up the low PV voltage to the level required for grid-connected and high-voltage applications [3–11].

The overall performance of renewable energy systems largely depends on the characteristics of the DC–DC converter, which serves as the interface between the energy source and the load by providing the required voltage conversion [12–14]. High step-up DC–DC converters are commonly classified into isolated and non-isolated



categories. Owing to their compact structure, reduced cost, and higher efficiency, non-isolated topologies are widely employed in practical applications. These converters include conventional boost converters, coupled-inductor-based converters, switched-capacitor converters, and multilevel converter topologies [15].

Among non-isolated converters, the conventional boost converter remains one of the most popular configurations because of its simple circuit structure, continuous input current, and single-switch implementation [16]. However, its voltage conversion capability is limited, and the main switch is exposed to high voltage stress when a large voltage gain is required. To overcome these shortcomings, coupled-inductor techniques have been widely introduced to enhance the voltage gain [17]. By properly selecting the coupled-inductor turns ratio together with the converter duty cycle, a significantly higher voltage conversion ratio can be achieved while maintaining operation in Continuous Conduction Mode (CCM). Nevertheless, the leakage inductance of the coupled inductor produces voltage spikes across semiconductor devices, leading to additional power losses and degraded converter performance. These adverse effects become increasingly significant as the turns ratio increases. Although snubber circuits are commonly employed to suppress these voltage transients, they cannot fully recover the energy stored in the leakage inductance [18,19]. Alternatively, active-clamp circuits effectively suppress voltage spikes and recycle the leakage energy; however, they increase the number of components, circuit complexity, and switching losses [20]. Consequently, passive-clamp techniques are often considered a more practical solution because they provide a simpler structure while maintaining low losses and satisfactory operating performance [21].

This paper presents a new quadratic high step-up DC–DC converter with a two-winding coupled-inductor configuration. The proposed structure achieves a high voltage conversion capability while maintaining a low component count, resulting in an improved voltage-gain-to-component ratio. In addition, it features low input current ripple, reduced voltage stress on the power switch, and efficient high step-up operation. Compared with conventional high-gain converter topologies, the proposed converter offers the following significant advantages:

- (1) **Extended Duty-Cycle Capability:** Unlike conventional Quasi-Z-Source (QZS) and Z-Source (ZS) converters, which operate within a restricted duty-cycle range, the proposed converter is capable of maintaining a high voltage conversion ratio over the entire duty-cycle operating region.
- (2) **Dual-Parameter Gain Adjustment:** The voltage gain can be independently determined by two design parameters: the converter duty cycle and the turns ratio of the coupled inductor. This dual-control capability provides greater design flexibility and facilitates adaptation to a wide range of operating conditions.
- (3) **High Step-Up Performance at Low Duty Cycles:** A high output voltage can be achieved without relying on extreme duty-cycle values. Operating at relatively low duty cycles reduces conduction losses and improves the overall efficiency and performance of the converter. **Low Voltage Stress on the Power Switch:** Owing to its quadratic voltage-boosting characteristic, the proposed topology significantly reduces the voltage stress experienced by the switching device. This feature enables the use of lower-rated semiconductor devices, decreases conduction losses, and contributes to higher system efficiency.
- (4) **Reduced Voltage Stress on the Switching Device:** Owing to its quadratic voltage-boosting characteristic, the proposed topology considerably lowers the voltage stress across the main switch. Consequently, lower-voltage-rated semiconductor devices can be employed, resulting in reduced power losses and enhanced conversion.

2. Proposed Topology

The circuit configuration of the proposed converter is shown in Figure 1. The topology employs a power switch (S), together with five diodes (D_1 – D_4 and D_o) and five capacitors (C_1 – C_4 and C_o). In addition, the converter incorporates two inductors (L_1 and L_2) and a two-winding coupled inductor consisting of a primary winding (N_p) and a secondary winding (N_s). The turns ratio of the coupled inductor is defined as $n = N_s/N_p$, while its magnetic coupling coefficient is expressed as $k = L_m/(L_m + L_k)$, where L_m and L_k denote the magnetizing and leakage inductances, respectively. Considering neglectable leakage inductance, we can assume that $k=1$. The equivalent structures and principal voltage and current waveforms of the proposed converter are presented in Figures 2 and 3., respectively.

First Mode: During this mode, the power switch (S) and diodes D_1 and D_3 are forward-biased, while diodes D_2 , D_4 and D_o are turned off. In this operating mode, the inductors L_1 and L_2 are charging. So, currents i_{L1} and i_{L2} increase linearly. The voltage relationships governing this interval can be derived using Kirchhoff's Voltage Law (KVL).

$$V_{N_s} = nV_{L_m} \quad (1)$$

$$V_1 = V_{L_m} + V_{L_k} \approx V_{L_m} \quad (2)$$

$$-V_{in} + V_{L_1} = 0 \quad (3)$$

$$-V_{in} + V_{L1} - V_{L2} + V_{C1} = 0 \quad (4)$$

$$V_{L2} + V_{C2} + V_1 - V_{C1} = 0 \quad (5)$$

$$-V_{C4} + V_{Ns} - V_{C3} + V_o = 0 \quad (6)$$

$$V_{Co} - V_o = 0 \quad (7)$$

$$V_{C1} - V_{L2} = 0 \quad (8)$$

Second Mode: During this mode, the power switch (S) is turned OFF, while diodes D_2 , D_4 , and D_o are forward-biased. The voltage relationships governing this interval can be derived using Kirchhoff's Voltage Law (KVL).

$$-V_{in} + V_{L1} + V_{C1} = 0 \quad (9)$$

$$-V_{C1} + V_{L2} + V_{C2} + V_1 = 0 \quad (10)$$

$$-V_{C4} + V_{Ns} = 0 \quad (11)$$

$$V_{Co} - V_o = 0 \quad (12)$$

Therefore, according to the relationships above:

$$V_{C1} = V_{C2} \quad (13)$$

$$V_{C3} = V_{C4} \quad (14)$$

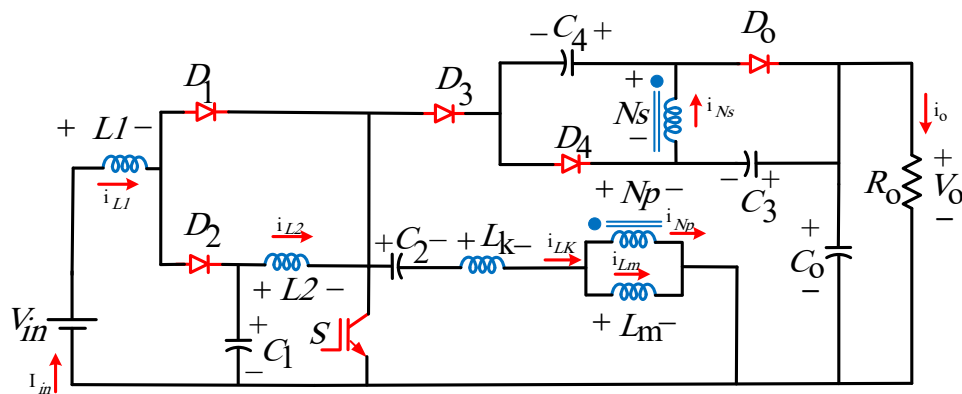


Figure 1. Power circuit of the proposed converter.

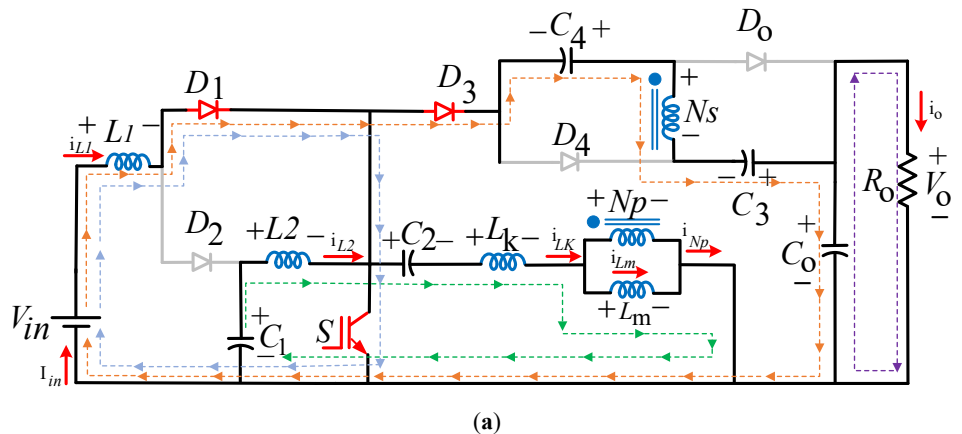


Figure 2. Cont.

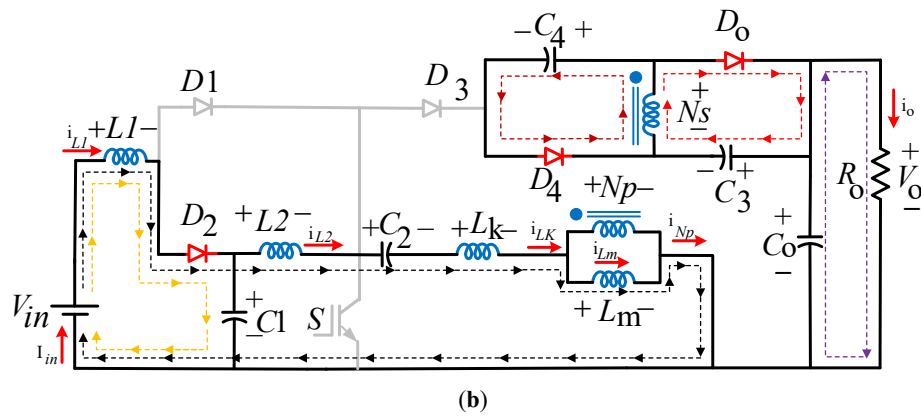


Figure 2. Equivalent structures of the proposed converter. (a) First mode, (b) Second mode.

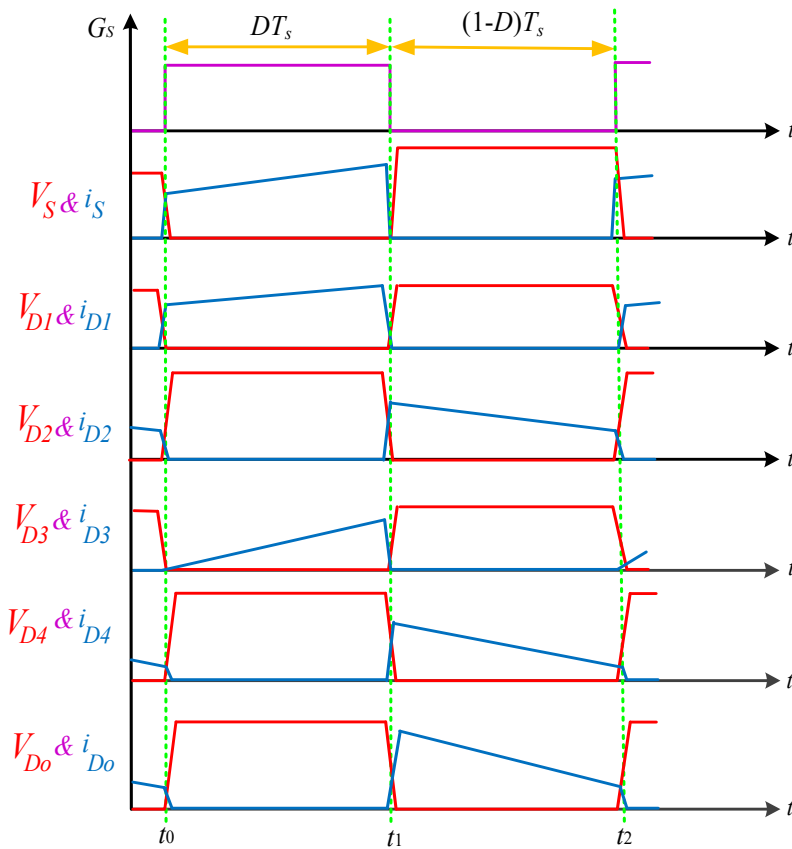


Figure 3. Main waveforms of the suggested converter.

2.1. Voltage Gain Calculation

The volt-second balance equations for the coupled inductor (CI) and inductor (L) are formulated as follows:

$$\langle V_{Lm} \rangle_{T_s} = 0 \quad (15)$$

$$\langle V_1 \rangle_{T_s} = 0 \quad (16)$$

$$\langle V_{L1} \rangle_{T_s} = 0 \quad (17)$$

$$\langle V_{L2} \rangle_{T_s} = 0 \quad (18)$$

The capacitor voltages are given in Equations (19) to (22):

$$V_{C1} = \frac{1}{1-D} V_{in} \quad (19)$$

$$V_{C2} = \frac{1}{1-D} V_{in} \quad (20)$$

$$V_{C3} = \frac{nD}{(1-D)^2} V_{in} \quad (21)$$

$$V_{C4} = \frac{nD}{(1-D)^2} V_{in} \quad (22)$$

The output voltage can be derived for the proposed topology as follows:

$$V_o = \frac{n(1+D)}{(1-D)^2} V_{in} \quad (23)$$

Considering ideal magnetic coupling ($k = 1$) for the coupled inductor, the output voltage gain is expressed as:

$$G = \frac{V_o}{V_{in}} = \frac{n(1+D)}{(1-D)^2} \quad (24)$$

2.2. Voltage Stresses of Semiconductors

The voltage stress across the power switch and diodes of the suggested converter can be expressed by:

$$V_S = \frac{V_{in}}{(1-D)^2} \quad (25)$$

$$V_{D1} = \frac{DV_{in}}{(1-D)^2} \quad (26)$$

$$V_{D2} = \frac{V_{in}}{1-D} \quad (27)$$

$$V_{D3} = \frac{(n-1)V_{in}}{(1-D)^2} \quad (28)$$

$$V_{D4} = \frac{nV_{in}}{(1-D)^2} \quad (29)$$

$$V_{Do} = \frac{nV_{in}}{(1-D)^2} \quad (30)$$

3. Comparison

A performance comparison is conducted between the proposed converter and several recently published high step-up DC–DC converter topologies to evaluate its effectiveness. The comparison is based on key design criteria, including voltage gain, voltage stress across the power switch, and the required number of circuit components. As presented in Table 1, the proposed topology is evaluated against the converters reported in [3–11,20,22,23]. The comparison reveals that the proposed converter achieves the highest voltage gain among the selected topologies in a wide range of duty cycles. To provide a clearer evaluation, the voltage gain characteristics of all converters are illustrated in Figure 4 for a coupled-inductor turns ratio of $n = 2$. In addition, Figure 5 and Table 1 indicate that the proposed topology imposes one of the lowest voltage stresses on the power switch, enabling the use of lower voltage-rated semiconductor devices, reducing switching and conduction losses, and consequently improving the overall converter efficiency. Furthermore, the final column of Table 1 identifies whether a common ground exists between the input source and the output load. This feature is highly desirable in renewable energy applications, as it simplifies system integration, reduces grounding issues, and facilitates practical implementation.

According to Table 1 and Figure 4, the converter in [5] employs the largest number of components, which may increase its implementation cost and power losses. Despite its high component count, it provides a relatively low voltage gain. However, the converter in [5] features a common ground between the input and output, making

it suitable for many renewable energy applications. In contrast, the converters in [7,8,11,22,23] do not share a common ground between the input and output, which may complicate their integration into certain renewable energy systems, particularly photovoltaic applications, and may increase common-mode electromagnetic interference (EMI), depending on the circuit configuration and grounding arrangement. In contrast, the proposed converter offers a suitable trade-off between voltage gain, voltage stress across the switches, and component count, making it a promising candidate for photovoltaic (PV) applications.

Table 1. Comparison with similar topologies.

Ref	Voltage Gain	Normalized Maximum Voltage Stress among All Switches ($V_{S,max}/V_o$)	Number of					Common Ground
			S	D	C	L	CI	
PC	$\frac{n(1+D)}{(1-D)^2}$	$\frac{1}{n(1+D)}$	1	5	5	2	1	Yes
[3]	$\frac{3-D}{1-D}$	$\frac{2}{3-D}$	2	5	4	3	0	Yes
[4]	$\frac{2D}{1-D}$	$\frac{1}{2D}$	1	2	3	2	0	Yes
[5]	$\frac{1+2D-2D^2}{(1-D)^2}$	$\frac{1}{1+2D-2D^2}$	1	5	6	4	0	Yes
[6]	$\frac{n+2D}{1-D}$	$\frac{1}{2+n(1+D)}$	1	4	5	1	1	Yes
[7]	$\frac{1+D}{(1-D)^2}$	$\frac{1}{1+D}$	1	4	4	3	0	No
[8]	$\frac{D(1+D)}{(1-D)^2}$	$\frac{1}{1+D}$	2	3	4	3	0	No
[9]	$\frac{2D(2-D)}{(1-D)^2}$	$\frac{1}{2D(2-D)}$	2	3	5	4	0	Yes
[10]	$\frac{(n+1)(2-D)}{1-D}$	$\frac{1}{(n+1)(2-D)}$	1	5	6	1	1	Yes
[11]	$\frac{D^2-4D+5}{(1-D)^2}$	$\frac{1}{D^2-4D+5}$	2	5	5	2	0	No
[20]	$\frac{n+1}{1-D}$	$\frac{1}{1+n}$	2	2	3	0	1	Yes
[22]	$\frac{1+3D}{1-D}$	$\frac{1}{1+3D}$	2	2	3	3	0	No
[23]	$\frac{3+2n+D}{1-D}$	$\frac{1}{3+2n+D}$	2	5	5	0	2	No

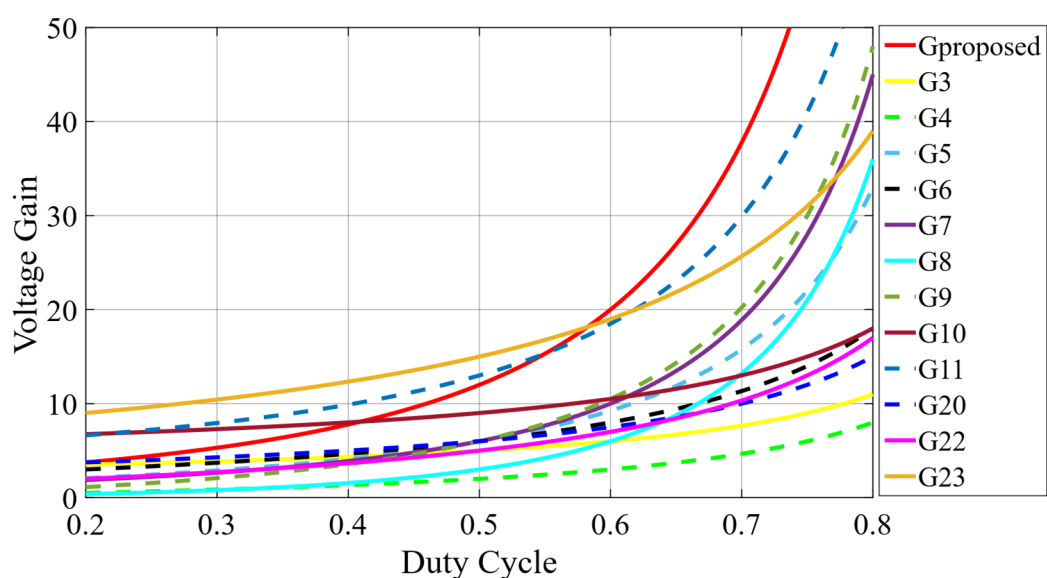


Figure 4. Comparison of voltage conversion ratios for the investigated boost converter topologies at various duty cycles.

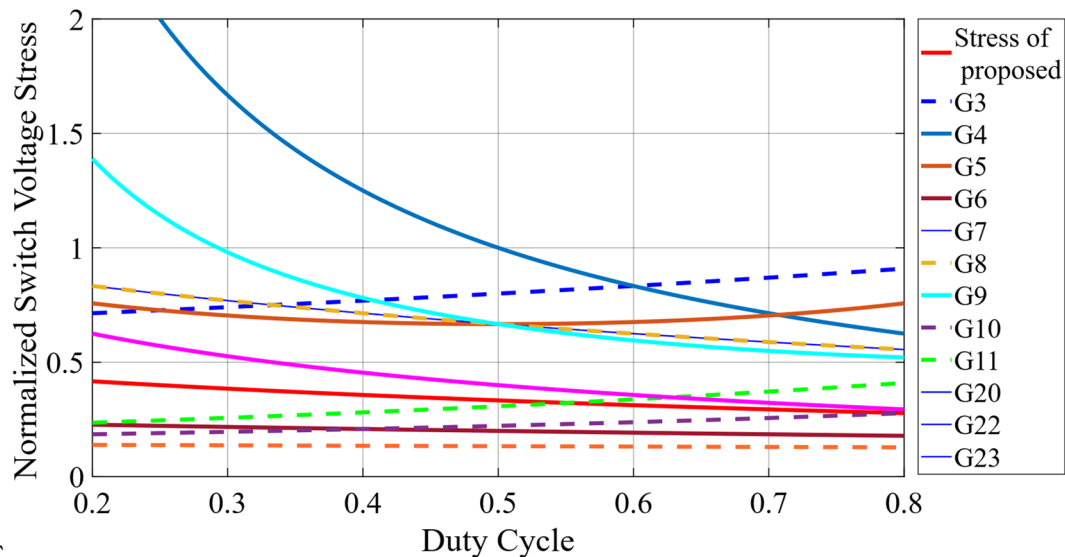


Figure 5. Comparison of the Normalized maximum voltage stress among all switches ($V_{S,max}/V_O$).

4. Simulation Results

The performance of the proposed converter is verified by comparing the analytical results with the corresponding simulation results, as presented in Figure 6a. Furthermore, all simulation results were obtained by considering the parasitic parameters of both the active and passive components. Therefore, the slight discrepancies between the simulation results and the analytical results are mainly attributed to these parasitic elements. The simulated output voltage is approximately 280 V, which closely matches the theoretical value of 280 V predicted by (23). The used parameters in simulation are summarized in Table 2. The excellent agreement between the analytical and simulation results confirms the accuracy of the derived mathematical model and validates the effectiveness of the proposed converter topology. The simulated voltage and current waveforms of the switch (S) are illustrated in Figure 6b. The voltage across the switch and the corresponding current are approximately 77 V and 8.9 A, respectively. Based on the analytical expression derived in (25), the theoretical switch voltage is 80 V, which shows excellent agreement with the simulation result, confirming the validity of the proposed analytical model. The simulated voltage and current waveforms of diode D_1 are presented in Figure 6c. The voltage across the diode is approximately 37 V, while the corresponding current is about 2.3 A. From the analytical result obtained using (26), the theoretical voltage stress of D_1 is 40 V, which is in close agreement with the simulation result, thereby confirming the accuracy of the theoretical analysis.

The simulated voltage and current waveforms of diode D_2 are illustrated in Figure 6d. The voltage stress across diode D_2 is approximately 36 V, and the corresponding current is about 2.4 A. According to the analytical expression in (27), The theoretical voltage stress is 40 V, which agrees well with the simulation result, demonstrating the validity of the proposed analytical model.

The simulated voltage and current waveforms of diode D_3 are shown in Figure 6e,f. The simulation results indicate a voltage stress of approximately 210 V, and the corresponding current is about 1.4 A. According to the analytical expression derived in (28), the theoretical voltage stress of D_3 is 240 V. The close agreement between the analytical prediction and the simulation result confirms the accuracy of the proposed theoretical analysis.

The voltage and current waveforms of diode D_4 obtained from the simulation are presented in Figure 6g,h. The voltage across diode D_4 is approximately 148 V, while the diode current is about 2.25 A. Based on the analytical formulation given in (29), the expected voltage stress is 160 V. The close correlation between the calculated and simulated values verifies the accuracy of the derived analysis and further validates the proposed converter topology. The parameters of the proposed converter are presented in Table 2.

Table 2. Proposed converter parameters.

Symbol	Description	Values
V_{in}	input Voltage	20 V
V_O	Output Voltage	280 V
D	Duty cycle	0.54
f_s	Switching frequency	50 kHz
R_o	Load resistance	600 Ω

Table 2. Cont.

Symbol	Description	Values
n	turns ratio, N_s/N_p	2
L_1, L_2	inductors	220 μH
L_m	Magnetizing	330 μH
L_k	Leakage inductor	2.8 μH
C_1	Capacitor	220 μF
C_2, C_3, C_4	Capacitors	68 μF
C_o	Capacitors	100 μF

The voltage and current waveforms of diode D_o are shown in Figure 6i,j. The voltage of diode D_o is approximately 142 V, while the diode current is about 1.5 A. Based on the analytical formulation given in (30), the expected voltage stress is 160 V. The close correlation between the calculated and simulated values verifies the accuracy of the derived analysis and further validates the proposed converter topology. The simulated capacitor voltages are illustrated in Figure 6k. The voltages of capacitors C_1 , C_2 , C_3 , C_4 , and C_o are approximately 38 V, -38 V, 76 V, 77.5 V, and 278 V, respectively. These values are in close agreement with the theoretical voltages calculated from (19)–(22), namely 40 V, 40 V, 80 V, 80 V, and 280 V. The consistency between analytical and simulation results further verifies the accuracy of the proposed converter analysis.

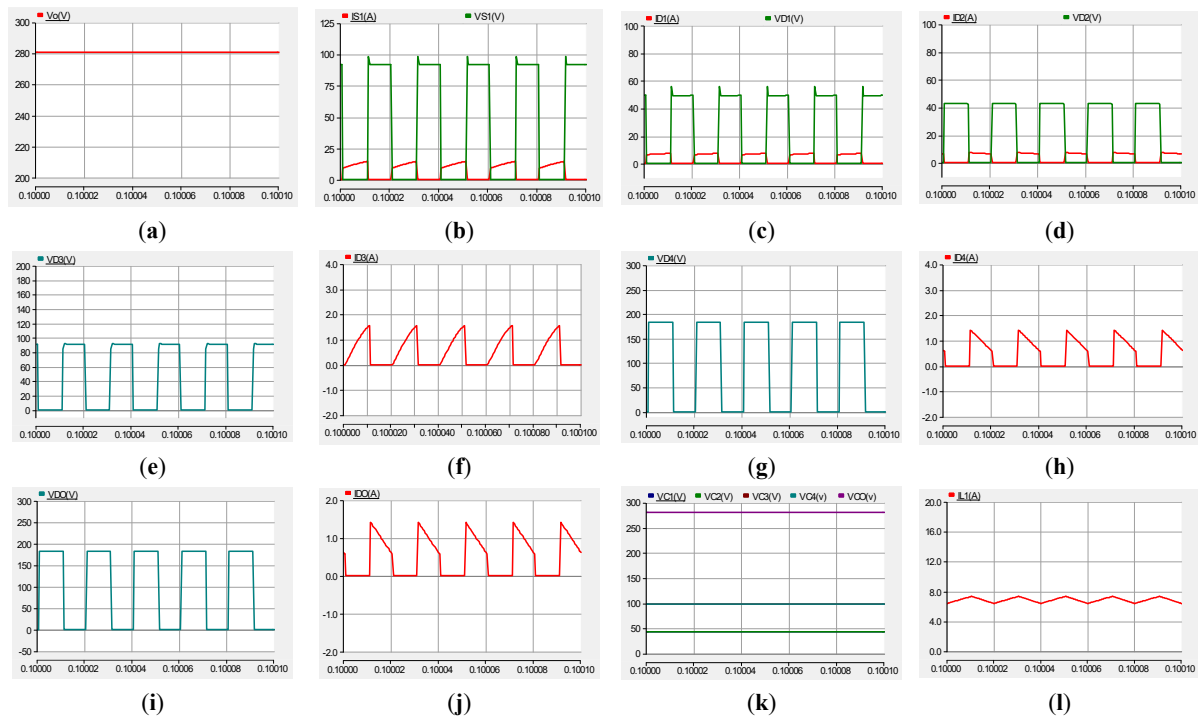


Figure 6. The simulation results of the proposed converter, (a) output voltage, (b) voltage and current of the switch (S), (c) voltage and current of diode D_1 , (d) voltage and current of diode D_2 , (e) voltage of diode D_3 , (f) current of diode D_3 , (g) voltage of diode D_4 , (h) current of diode D_4 , (i) voltage of diode D_o , (j) current of diode D_o , (k) voltage of the capacitors C_1 , C_2 , C_3 , C_4 and C_o , (l) input current.

Figure 6l shows the input current waveform of the proposed converter. As can be observed, selecting a sufficiently large value for inductor L_I results in a low input-current ripple, which is a desirable feature for photovoltaic (PV) applications.

Figure 7 illustrates the non-ideal voltage gain of the proposed converter as a function of the duty cycle. This curve was obtained by simulating the proposed converter under non-ideal operating conditions, taking into account the parasitic parameters of the active and passive components, and extracting the corresponding voltage-gain values over the considered duty-cycle range. As can be observed, the voltage gain decreases significantly at high duty cycles because of the rapidly increasing power losses associated with the parasitic elements. This behavior indicates that operating the proposed converter at excessively high duty cycles is impractical. Therefore, the converter is more suitable for operation within a moderate duty-cycle range, where a more favorable trade-off between voltage gain and power losses can be achieved.

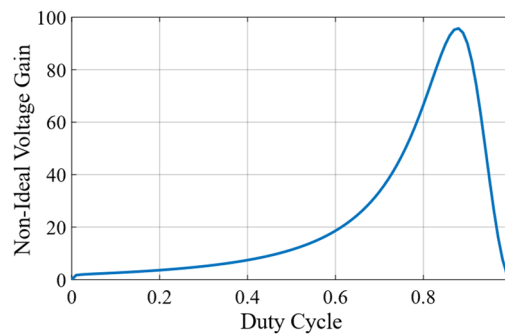
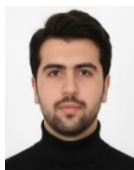


Figure 7. Non-ideal voltage gain of the proposed converter.

5. Conclusions

This article introduces the development and analysis of a new quadratic high step-up DC–DC converter employing a single-switch configuration. This topology is characterized by a high voltage gain, low input current ripple, low switch voltage stress, a common ground structure, and enhanced flexibility in gain adjustment through both the duty cycle and the coupled-inductor turns ratio. The converter offers several advantageous features, including a high voltage boosting capability, reduced switch voltage stress, a common ground between the input and output terminals, and flexible gain adjustment through two independent parameters. Furthermore, the single-switch structure eliminates the duty-cycle limitations commonly encountered in conventional high-gain converters, enabling significant voltage amplification even at relatively low duty cycles. The proposed converter is well suited for applications such as photovoltaic systems, renewable energy systems, and DC microgrids.

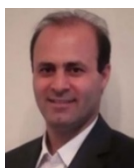
6. Biographies of the Authors



Ali Taghipour Jamshidi was born on 30 March 2001, in Tabriz, East Azerbaijan, Iran. He received the B.Sc. degree in Electrical Power Engineering from the University of Tabriz on 2023. Currently he is studying Master in Power Electronics at University of Tabriz, Department of Electrical and Computer Engineering. His research interest includes power electronics, DC–DC converters, DC–AC converters, AC–AC converters, Z-source converters and their applications.



Pedram Panahporian born in Tabriz in 2000. He Received the B.E. degree in Electrical Engineering from Shahid Madani Azarbaijan University, Tabriz, Iran, on 2023. Currently he is working as a Master student in Power Electronics and he is also working on electrical projects any activities related to electronic and computer engineering. His current research interests include boost converters, inverters, and power electronics converters and their applications in renewable energy.



Ebrahim Babaei received the Ph.D. degree in electrical engineering from the University of Tabriz, Tabriz, Iran, in 2007. In 2007, he joined the Faculty of Electrical and Computer Engineering, University of Tabriz. He has authored and coauthored one book, two book chapters, and more than 800 journal and conference papers. He also holds 26 patents in the field of power electronics. His current research interests include the analysis, modeling, design, and control of power electronics converters and their applications, renewable energy sources, and FACTS devices. Dr. Babaei has been the Editor-in-Chief of the Journal of Electrical Engineering at the University of Tabriz since 2013. He served as an Associate Editor of IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS from 2015 to 2023. Currently, he is an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE OPEN JOURNAL OF THE INDUSTRIAL ELECTRONICS SOCIETY, Iranian Journal of Science and Technology, Transactions of Electrical Engineering, and the International Journal of Circuit Theory and Applications. He has also acted as the Corresponding Guest Editor for two special issues of IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS. In addition, he has held roles such as Technical Program Chair, Track Chair, organizer of various special sessions, and Technical Program Committee member in major international conferences in the field of power electronics. He was the recipient of the Best Researcher Award multiple times from the University of Tabriz and the 2016 Outstanding Reviewer Award from the IEEE Transactions on Power Electronics (honored as a Prize Winner). In 2022, the Ministry of Science, Research and Technology recognized him as a distinguished Researcher of Iran in engineering.



Mehran Sabahi was born in Tabriz, Iran. He received the B.S. degree in Electronic Engineering from the University of Tabriz, Iran, the M.S. degree in Electrical Engineering from Tehran University, Tehran, Iran, and the in Electrical Engineering from University of Tabriz, in 1991, 1994, and 2009, respectively. In 2009, he joined the faculty of Electrical and Computer Engineering, University of Tabriz. He was an Assistant Professor since 2009 to 2013 and has been Associate Professor since 2014. His current research interests include the power electronics in renewable systems.



Seyed Hossein Hosseini was born in Marand, Iran, in 1953. He received the M.S. degree (Hons.) in electrical engineering from the Faculty of Engineering, University of Tabriz, Tabriz, Iran, in 1976, and the D.E.A. (Hons.) and Ph.D. degrees in electrical engineering from Institute National Polytechnique de Lorraine, Nancy, France, in 1978 and 1981, respectively. In 1982, he joined the Department of Electrical Engineering, University of Tabriz, as an Assistant Professor. From September 1990 to September 1991, he was a Visiting Professor with The University of Queensland, Brisbane, Australia. From 1990 to 1995, he was an Associate Professor with the University of Tabriz, where he has been a Full Professor with the Department of Electrical Engineering, since 1995. From September 1996 to September 1997, he was a Visiting Professor with the University of Western Ontario, London, ON, Canada. Since January 2017, he has been a Professor with Near East University, North Cyprus, Turkey. He has authored more than 700 journal articles and conference papers.

Author Contributions

A.T.J.: conceptualization, formal analysis, investigation, methodology, validation, writing—original draft, writing—review and editing; P.P.: conceptualization, formal analysis, investigation, methodology, validation, writing—original draft, writing—review and editing; E.B.: formal analysis, investigation, methodology, supervision, validation, writing—review and editing; M.S.: formal analysis, investigation, methodology, supervision, validation, writing—review and editing; S.H.H.: formal analysis, investigation, methodology, supervision, validation, writing—review and editing. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest

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Use of AI and AI-Assisted Technologies

No AI tools were utilized for this paper.

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