

Optimal Switched-Capacitor Network for Synchronized Multiple Bias-Flip Piezoelectric Energy Harvesting Circuit

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Abstract: Synchronized multiple bias-flip (SMBF) techniques improve power harvesting capability for piezoelectric energy harvesting (PEH), yet generating optimal multi-level bias voltages with minimal passive components remains challenging. This paper proposes an optimal reconfigurable switched-capacitor network for SMBF interfaces. By reconfiguring and reusing flying capacitors, up to 27 successive bias-flip actions (S27BF) are realized using only five capacitors. Owing to the symmetric bias-flip operations, the flying capacitors can maintain their bias voltages without auxiliary power sources. A discrete printed circuit board (PCB) prototype validates the design. Experimental results show that the S27BF circuit yields 3.89-fold peak harvested power compared with the standard full-bridge rectifier benchmark, even with a low-quality-factor inductor. Practical limitations including piezoelectric dielectric loss and diode voltage drop are also discussed. This work provides further physical insight into PEH research and offers a feasible hardware solution for high-order SMBF implementations.

Keywords: energy harvesting; piezoelectric; synchronous switch interface circuit

1. Introduction

The ambient environment contains abundant distributed kinetic, thermal, and light energy. Such energy can be converted into electricity by leveraging localized micro-transducers. Over the past two decades, energy harvesting (EH) and power management (PM) technologies have advanced rapidly. Concurrently, modern ultra-low-power electronics have significantly reduced the operational energy requirements of Internet of Things (IoT) nodes [1,2]. As the gap between ambient power generation and local consumption continues to narrow, self-powered IoT systems have become increasingly feasible. This reduces the dependence on conventional electrochemical batteries and the associated maintenance costs. It also mitigates the environmental impact of disposing of large quantities of chemical batteries.

Kinetic energy has been extensively studied as one of the promising candidates in ambient EH. There are some early commercially available products, such as kinetic-powered light switches [3]. There are also some development platforms based on EH-IoTs such as ViPSN [4]. In kinetic EH, three types of electromechanical transducers are most commonly employed. They include electromagnetic transducers, electrostatic transducers, and piezoelectric transducers. Among these types, piezoelectric transducers provide relatively high output voltage with straightforward processability. Their mechanical configuration is compact. Thus, they are relatively simple to fabricate. Due to these merits, piezoelectric structures have been extensively studied for battery-free IoT applications.

Piezoelectric materials produce charge migration and electric potential when mechanical strain is applied. Natural vibration-induced strain enables piezoelectric transducers to output AC voltage. Interface circuits are required to convert piezoelectric output AC voltage into stable and regulated DC form. The full-bridge rectifier (FBR), which is also referred to as the standard energy-harvesting (SEH) circuit, is the most typical interface circuit for such a rectification task. It is widely recognized as the benchmark in numerous studies on piezoelectric energy harvesting (PEH) interface circuits [5–7]. On the other hand, since the output impedance of a piezoelectric transducer

is capacitive, the current and voltage of the piezoelectric transducer are in quadrature under open-circuit condition. The phase difference decreases when an SEH interface circuit is employed. However, the voltage still lags the current by less than 90° . That is, the output impedance falls between purely resistive and purely capacitive. In this scenario, at first glance, the compensation concept is readily adopted by leveraging the conventional thought in power electronics. Connecting an inductive load cancels the negative imaginary component of the capacitive impedance. Nevertheless, this configuration is not practically implementable in engineering applications. The piezoelectric capacitance is mostly on the nanofarad scale. Meanwhile, the mechanical vibration frequencies of most piezoelectric structures are below 100 Hz. Thus, the matched inductance should be in the tens or even hundreds of henries. Such inductors exhibit a large physical size. This size is huge compared with that of small-scale piezoelectric energy harvesters.

Unlike the conventional linear-impedance compensation concept, the synchronous electric charge extraction (SECE) technique adopts a small-size switch circuit. This synchronous switching circuit also achieves an equivalent compensation effect. This technique was first proposed in 2005 [8]. It extracts the energy stored in the piezoelectric capacitor at specific instants of maximum or minimum voltage/charge. Through transient manipulation of the voltage waveform, the piezoelectric voltage is maintained in phase with the equivalent current source. The proposed technique actively compensates the output impedance. It significantly reduces the requirement for large inductors. Other advantages, such as load-independent power output and inductor-sharing for array-based PEH, render it a promising candidate in PEH applications.

Besides the SECE technique, the synchronized switch harvesting (SSH) technology is also applied to modify the SEH interface circuit for PEH enhancement. In parallel synchronized switch harvesting on inductor (P-SSHI), an inductive switching branch forms a transient resonant loop with the intrinsic piezoelectric capacitance [9]. The LC circuit rapidly inverts the transducer voltage at synchronized voltage extrema, thereby extending the subsequent rectifier-conduction interval. Compared with SECE, P-SSHI retains the rectification-based energy-transfer path. It enhances the harvested power via synchronized voltage inversion. However, its harvested power is dependent on the load resistance. Compared with SECE, more circuit modules, such as maximum power point tracking (MPPT), are required for maintaining a high harvested power. A voltage-flipping ratio closer to -1 leads to better energy harvesting performance. The achievable voltage-flipping ratio is primarily determined by the quality factor of the LC resonant loop, which is influenced by the equivalent series resistance (ESR) of external inductor and switching network.

Since the synchronized-switch technique was proposed, numerous energy-harvesting interface circuits based on synchronized switching with distinct working principles have been developed, such as (series SSHI) S-SSHI [5] and synchronous inversion and charge extraction (SICE) [6]. Meanwhile, researchers have continuously improved P-SSHI. Beyond conventional single-step SSHI, multi-step bias-flip techniques have been investigated to further improve the voltage inversion efficiency. By introducing multiple intermediate bias-voltage levels during the flipping process, the voltage profile of the piezoelectric transducer can be more closely shaped toward the optimal profile in the infinite- Q limit. Wang et al. [10, 11] proposed a high-efficiency multi-step bias-flip interface, which adopts multiple intermediate bias voltages. It enhances the voltage-flipping process. Meanwhile, it reduces the reliance on a single resonant transition. Current research trends mainly focus on two aspects.

- Enhancing the circuit's voltage-waveform manipulation capability to further increase the conduction angle.
- Minimizing or eliminating the need for an inductor to reduce the system size and enable partial or full integration of the interface circuit.

From a circuit perspective, P-SSHI realizes a single-step inductive bias flip. To reduce the dependence on a high- Q external inductor, capacitor-based and hybrid capacitor–inductor bias-flip techniques have subsequently been developed.

An inductor-only solution and other capacitor-collaborative alternatives for voltage bias flipping are depicted in Figure 1. To realize an inductor-free design, synchronized switch harvesting on capacitor (SSHC) is proposed [12]. Several capacitors are connected to the network in a specific order. They perform charge exchange among the piezoelectric capacitor and all flying capacitors. The design target is to flip the piezoelectric voltage with minimal energy dissipation. Ref. [13] uses multiple capacitors to form an array and divides the flipping process into multiple steps. This approach reduces the total energy dissipation introduced by the switching current via a series of voltage levels, which are produced by the connected flying capacitors. Another option for realizing efficient voltage bias flip utilizes a series-connected inductor and a flying capacitor network. During each bias-flipping process, a C_p - L_i - C_b resonant loop is formed. C_p denotes the piezoelectric capacitor. L_i is an inductor dedicated to voltage inversion/flip. C_b consists of flying capacitors in the array. It provides a specific bias voltage. With an organized switching sequence of bias-flip actions, the requirement for a high-quality-factor inductor in P-SSHI is significantly alleviated. The use of switched-capacitor networks enables the voltage-flipping operation to be implemented with smaller passive components and provides additional flexibility in generating intermediate bias-voltage levels.

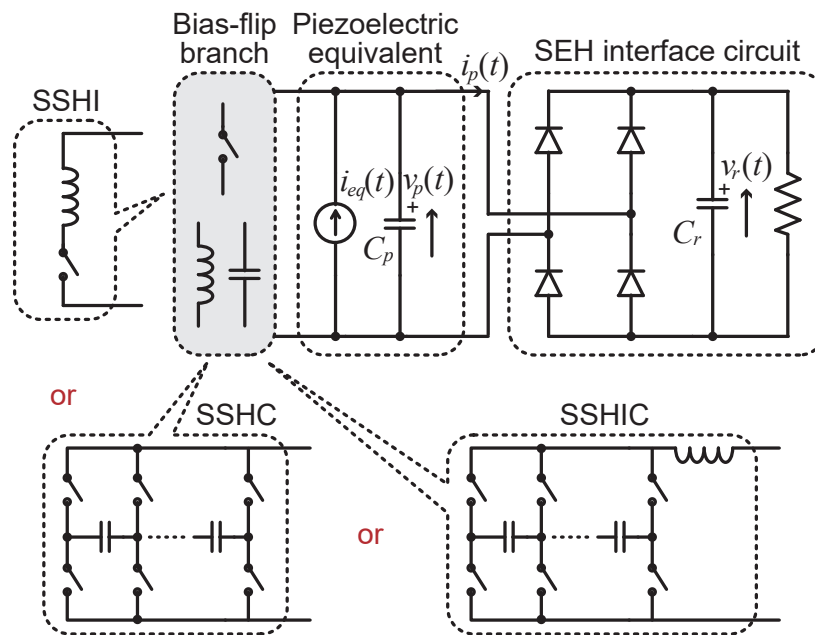


Figure 1. Circuit Topologies of SSHI, SSHC, and SSHIC for PEH enhancement.

The switched-capacitor approach has also attracted significant attention because it enables the implementation of PEH interfaces without bulky external inductors. Xie et al. proposed a fully integrated frequency-tuning switched-capacitor rectifier for PEH. This work highlights the potential of switched-capacitor techniques in developing compact and integrated EH interface circuits [14]. Hybrid capacitor–inductor interfaces offer another approach to reducing passive-component size in PEH systems [15]. The C-L-C resonant loop has also been applied to multiple bias-flip circuits. Ref. [16] further explored a bias-flip interface combining switched capacitors and an inductor for piezoelectric and RF energy harvesting. Under the same flying-capacitor network configuration, experimental results demonstrate that the C-L-C scheme of the SSHIC circuit outperforms the C-C charge-exchange scheme of its SSHC counterpart. A further step toward reducing the passive-component overhead is to reuse capacitors that already serve other functions in the PEH system. Yue and Du proposed a synchronized-switch harvesting on shared capacitors (SSHSC) rectifier [17]. Three energy-storage capacitors with a 3 : 3 : 1 capacitance ratio are reused as flying capacitors during the bias-flip operation in this rectifier. This capacitor-sharing technique eliminates dedicated flying capacitors. It reduces the required circuit area and the number of interface connections. This result demonstrates that capacitor reuse can provide an additional degree of freedom for designing compact SSHC interfaces. Yue et al. proposed a fully integrated sequential SSHC rectifier based on a split-electrode piezoelectric transducer [18]. This rectifier cyclically performs synchronized voltage flipping on multiple sub-transducers in sequence. By sequentially reusing the flying capacitors, the proposed architecture achieves capacitor sharing. It maintains high voltage-flipping efficiency and enables full on-chip implementation. In contrast to previous capacitor-reuse techniques that primarily target component sharing and circuit-area reduction, this work focuses on maximizing the number of bias-flip actions achievable with a fixed number of flying capacitors.

Beyond case studies with different flying-capacitor networks, a mathematical model of synchronized multiple bias flip (SMBF) was developed to generalize the optimal operating conditions [19]. Based on this theoretical model, voltage-flipping operations are implemented sequentially via a set of optimal DC voltage biases, allowing capacitors to serve as self-adaptive DC bias sources. Several practical implementations, including P-S3BF, S-S3BF, and P-S7BF, have subsequently been developed [20–22]. These implementations experimentally demonstrate that increasing the number of properly designed bias-flip actions can further improve the PEH performance.

Recent IC implementations have further explored capacitor reuse and reconfiguration to increase the number of effective voltage-flipping phases. Wang et al. proposed a collaborative-flip SSHC rectifier. This rectifier reuses shared capacitors to increase the number of flipping phases. It improves the voltage-flipping efficiency under appropriate capacitance conditions [23].

Recent developments demonstrate that the achievable number of bias-flip phases is strongly related to the configuration and reuse of available capacitors. However, existing implementations generally rely on topology-specific capacitor configurations. The relationship between the number of available capacitors and the maximum achievable number of bias-voltage levels or bias-flip actions has not been systematically established. Thus, the key design question is how to maximize the number of effective bias-flip actions using a fixed and limited number of capacitors.

To address this problem, this paper develops an optimal switched-capacitor-array configuration for synchronized multiple bias-flip PEH. By systematically reconstructing and reusing a limited number of capacitors via different series-parallel combinations, the proposed architecture maximizes the number of available bias-voltage levels. It enables 27 successive bias-flip actions with five capacitors. The proposed design also relaxes the quality-factor requirement of the resonant inductor while retaining a simple gate-driving scheme. A discrete-component prototype is implemented to experimentally validate the proposed capacitor configuration and bias-flip sequence. Experimental results demonstrate the power-enhancement benefit of increasing the number of bias-flip actions while also revealing diminishing practical returns as the number increases further.

2. Principle of PEH and SSH Circuits

Figure 2a shows the equivalent circuit model of the piezoelectric transducer under constant force magnitude excitation [9]. $nv_{eq}(t) = -M\ddot{y}(t)$ is the equivalent voltage source. $-M\ddot{y}(t)$ denotes the inertial force equivalently applied by the base movement $y(t)$. n represents the electromechanical coupling coefficient or equivalent turn ratio in the equivalent transformer model. $D = n^2 R_m$ is the mechanical damping coefficient. It is equivalent to the resistor R_m in electrical domain. Similarly, M and K are mechanical mass and stiffness, respectively. Their electrical equivalents are inductor L_m and capacitor C_m , respectively. The short-circuit (eliminating the effect of electrical part) resonant frequency of the piezoelectric vibrator is expressed as $\omega_0 = \sqrt{K/M} = 1/\sqrt{L_m C_m}$. In the electrical domain, C_p is the inherent piezoelectric clamped capacitance, i.e., the capacitance measured under zero displacement boundary condition. R_p is the parasitic resistance representing the effect of dielectric loss. It is usually relatively large, reaching hundreds of M Ω , and, therefore, neglected in many studies.

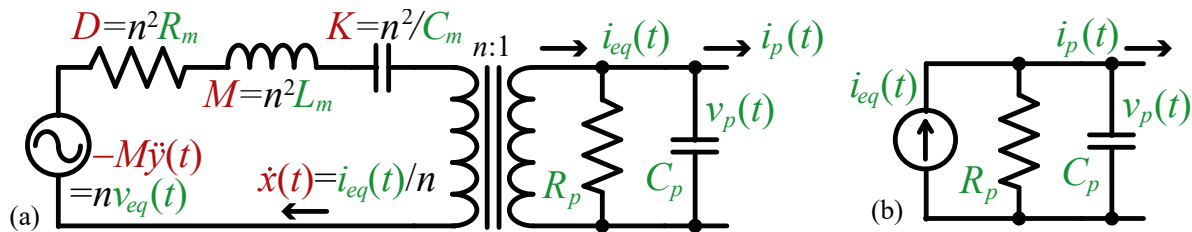


Figure 2. Equivalent circuit of a piezoelectric transducer. Mechanical parameters in red. Electrical parameters in green. (a) Under constant force magnitude excitation. (b) Under constant displacement magnitude excitation.

When the system is excited under constant displacement magnitude excitation or under weakly coupled cases, i.e., the electrical loading conditions hardly influence the mechanical dynamics, the equivalent circuit can be reduced to the one shown in Figure 2b. In the simplified equivalent circuit, a current source i_{eq} is connected in parallel with the piezoelectric capacitance C_p and dielectric equivalent resistance R_p . i_{eq} is proportional to the vibration velocity $\dot{x}$. $\dot{x}$ denotes the relative velocity of the equivalent mass with respect to the vibrating base. The current-source reduced model is widely adopted in circuit design and analysis. It helps eliminate or decouple complex electromechanical-coupling dynamics. This enables circuit designers to focus on the circuit itself. The analysis is performed under relatively simple boundary conditions.

This paper discusses the circuit design under constant displacement magnitude excitation. Under this excitation, the equivalent current source i_{eq} generated by harmonic excitation is illustrated in Figure 3. It is formulated as follows.

$$i_{eq}(t) = I_{eq} \sin(\omega_0 t). \quad (1)$$

Consider the P-SSHI circuit illustrated in Figure 1. The SEH module rectifies the AC voltage generated by the transducer. It stabilizes the output voltage using a filtering/storage capacitor. The filtering/storage capacitor C_r is usually selected much larger than the piezoelectric capacitor C_p . Thus, v_r is considered a constant DC voltage in each vibration cycle. Figure 3 shows the voltage and current waveforms in P-SSHI. When the diode bridge conducts, the current source delivers energy to C_r . At the instant t_f , when $i_p(t_f) = 0$, the diode bridge transitions from forward conduction to reverse blocking. At this moment, the P-SSHI circuit operates. It inverts the polarity of v_p , the voltage across C_p , i.e., from V_r to γV_r , as shown in Figure 3b. The parameter γ denotes the ratio of the piezoelectric voltage immediately after inversion to that immediately before inversion in the interface treatment. In a bias-flip action, by utilizing the switched L_i - C_p circuit, a transient voltage change is realized. The voltage flipping ratio is formulated as follows

$$\gamma \approx -e^{-\pi/(2Q)}, \quad (2)$$

where $Q = \sqrt{L_i/C_p}/r$ denotes the quality factor of the L_i - C_p circuit. r represents the ESR of the circuit, which includes the inductor ESR and MOSFET on-resistance in the transient resonant loop.

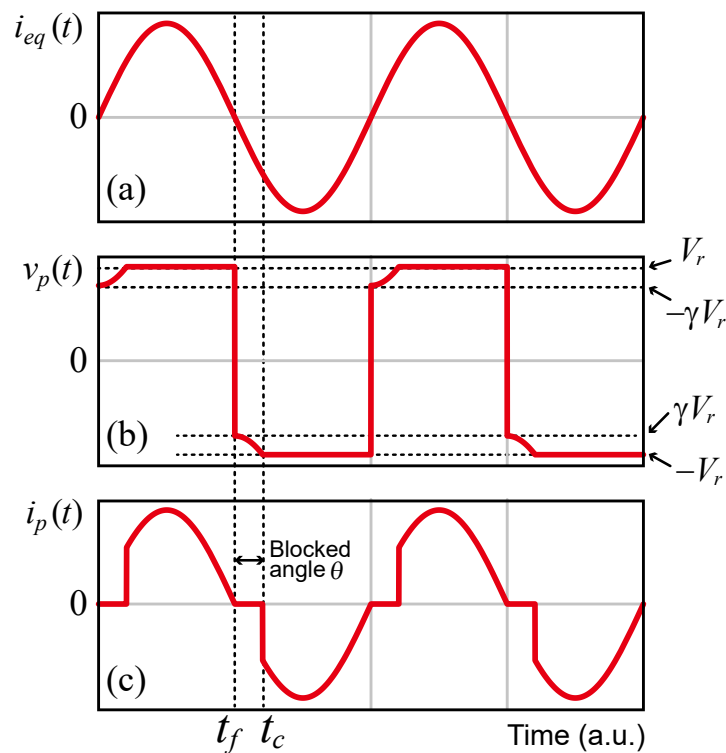


Figure 3. Typical voltage and current waveform in P-SSHI.

After t_f , $i_{eq}(t)$ continues to charge C_p . The charging process persists until the diode bridge conducts again at time t_c . If there is no bias-flip action, i.e., in the SEH case, this corresponds to $\gamma = 1$. In the ideal flipping case, where $Q = \infty$, we have $\gamma = -1$. In all the $\gamma \leq 0$ cases, the conduction angle of the diode bridge is 180° in each half cycle, i.e., the diode bridge is always in conduction.

The average harvested power is calculated over the positive-current conduction interval preceding t_f , i.e.,

$$P_h = \frac{\omega_0}{\pi} V_r \int_{t_c - \pi/\omega_0}^{t_f} I_{eq} \sin(\omega_0 t) dt. \quad (3)$$

Denoting the rectifier blocked angle in a half cycle as θ , as shown in Figure 3c, we have

$$\cos \theta = \cos [\omega_0(t_c - t_f)] = 1 - (1 + \gamma)\tilde{V}_r, \quad (4)$$

where

$$\tilde{V}_r = \frac{V_r}{V_{oc}} = V_r / \left(\frac{I_{eq}}{\omega_0 C_p} \right) \quad (5)$$

is the rectified voltage normalized by the open-circuit voltage V_{oc} . Substituting (4) and (5) into (3) gives the ultimate expression of the average harvested power

$$P_h(\tilde{V}_r) = \frac{I_{eq}^2}{\pi \omega_0 C_p} \tilde{V}_r [2 - (1 + \gamma)\tilde{V}_r]. \quad (6)$$

From (6), P_h is a downward-opening quadratic function with respect to $\tilde{V}_r$. Taking the first-order derivative of P_h with respect to $\tilde{V}_r$ and setting it to zero yields

$$\frac{dP_h}{d\tilde{V}_r} = \frac{I_{eq}^2}{\pi \omega_0 C_p} [2 - 2(1 + \gamma)\tilde{V}_r] = 0. \quad (7)$$

The optimal normalized load voltage is therefore

$$\tilde{V}_{r,\text{opt}} = \frac{1}{1+\gamma}. \quad (8)$$

Substituting $\tilde{V}_{r,\text{opt}}$ back into (4), we obtain

$$\cos(\theta_{\text{opt}}) = 0 \Rightarrow \theta_{\text{opt}} = \frac{\pi}{2}. \quad (9)$$

The maximum harvested power is given by

$$P_{h,\text{max}} = \frac{I_{eq}^2}{\pi\omega_0 C_p} \frac{1}{1+\gamma}. \quad (10)$$

As can be seen from (8)–(10), the optimal blocking angle $\theta_{\text{opt}} = \pi/2$ is independent of the voltage flipping ratio γ , whereas both the optimal normalized voltage $\tilde{V}_{r,\text{opt}}$ and maximum harvested power $P_{h,\text{max}}$ explicitly depend on γ . Smaller γ , i.e., more ideal flipping toward -1 , leads to a larger rectified voltage and enhances the maximum harvestable power.

SEH can be taken as a special case of P-SSHI, where $\gamma = 1$. The results on harvested power agree with the classical analysis in literature [7]. The short-circuit P-SSH harvesting circuit reported in [24] can be taken as $\gamma = 0$. In implementations reported in the literature, the utilized practical inductors in P-SSHI circuit usually can achieve a flipping factor $\gamma = -0.5$ to -0.7 . Given $V_{oc} = 5$ V, Figure 4 presents the variation trend of harvested power P_h in a specific scenario as a function of rectified voltage V_r and flipping/inversion factor γ . It intuitively indicates that optimizing the flipping/inversion factor toward the ideal value of -1 significantly enhances the harvested power.

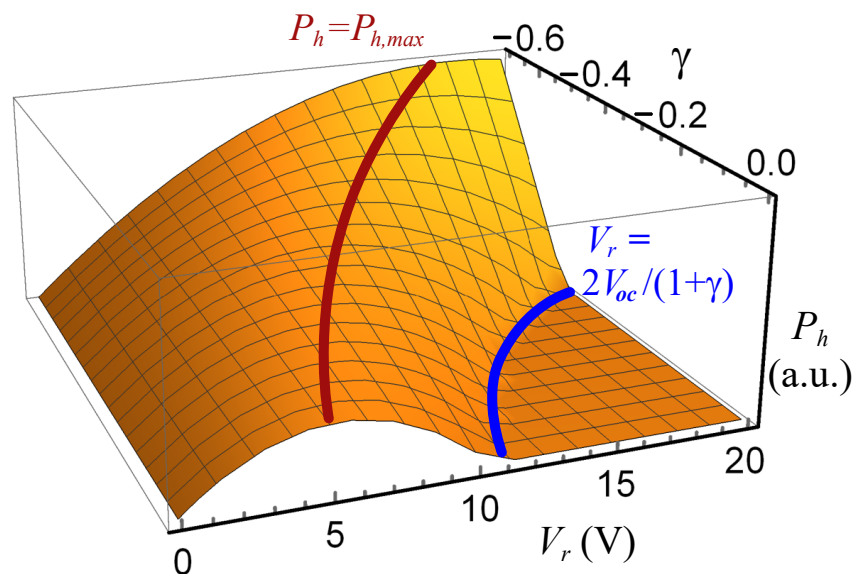


Figure 4. Harvested power in P-SSHI under different rectified voltage V_r and flipping factor γ . ($V_{oc} = 5$ V).

3. Conceptual SMBF Circuit

The conventional P-SSHI performs only one bias-flip action at each synchronized voltage peak. This action corresponds to a zero-bias flipping strategy. To further improve energy extraction capability, subsequent studies explored the feasibility of implementing multiple successive bias-flip operations within one synchronized instant. This exploration led to various multiple-step bias-flip topologies, which can be summarized by the SMBF model [19,20,22].

Figure 5 presents a conceptual parallel SMBF (P-SMBF) circuit model. P-SMBF is categorized as an advanced version of the P-SSHI interface circuit. The bias-voltage network is modified from a single zero-volt bias in SSHI to multiple bias voltages in SMBF. The two diodes with forward voltage V_{ds} passively achieve zero current switching (ZCS). ZCS is realized when the inductor current returns to zero. It helps reduce the timing and control complexity. The synchronized switch actions are carried out at the same instants as SSHI does, i.e., the zero crossing point of the piezoelectric current. Unlike the SSHI technique, which performs only one bias-flip operation at each synchronization instant, the SMBF method flips the piezoelectric voltage sequentially with respect to M bias-voltage sources, i.e., from $V_{b,1}$ to $V_{b,M}$ as illustrated in Figure 5. During each bias-flip action, C_p , L_i , r , a specific bias

source $V_{b,m}$, and the current-steering diode form an RLC resonant circuit. This circuit enables rapid flipping of the piezoelectric voltage relative to $V_{b,m}$. Figure 6 shows the equivalent circuit and voltage waveform in one voltage bias-flip action. The time constant of an electrical LC circuit is much smaller than that of a mechanical piezoelectric structure. When i_{eq} crosses zero, the transient change of v_p occurs almost instantaneously.

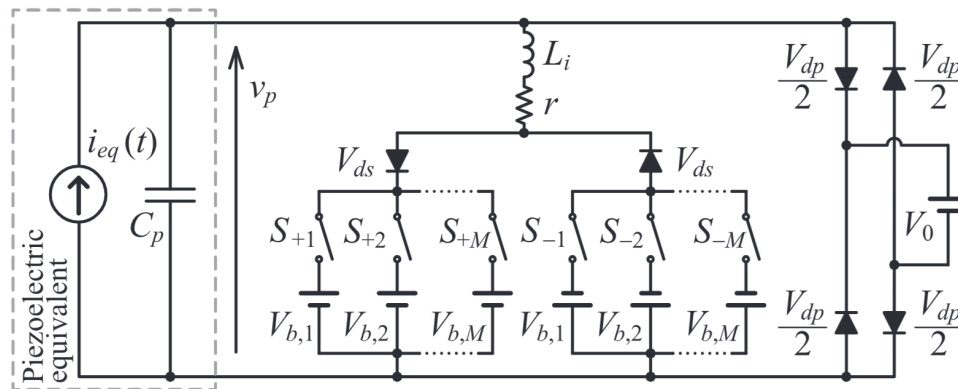


Figure 5. Conceptual multiple bias-voltage model for explaining the P-SMBF operation [19].

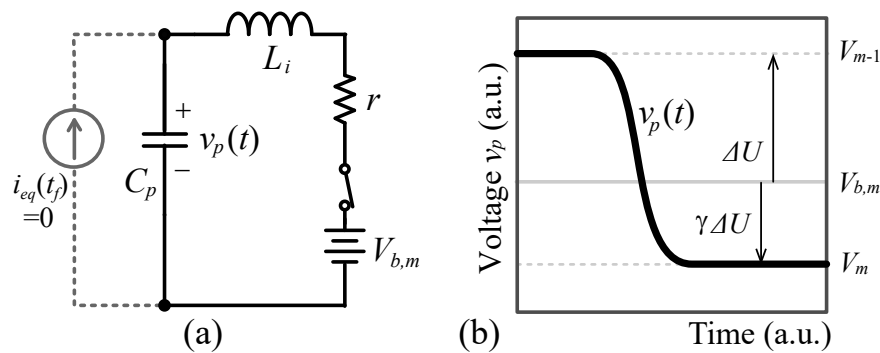


Figure 6. A single voltage bias-flip action in SMBF circuit. (a) Equivalent circuit. (b) Voltage waveform.

Through closed-form analysis [19], the general SMBF model reveals that, under the optimal operation leading to maximum harvested power, all DC bias voltages satisfy the following two characteristics:

- The optimal DC bias voltages are symmetrically distributed with respect to zero;
- The voltage changes in all bias-flip actions are the same.

Mathematically,

$$\begin{cases} V_{b,m} = -V_{b,M-m+1}, & \forall m = 1, 2, \dots, M; \\ V_{b,m-1} - V_{b,m} = (1 - \gamma)\Delta U. & \forall m = 2, 3, \dots, M. \end{cases} \quad (11)$$

Given these M bias voltage sources, the $M + 1$ transition piezoelectric voltages in a series of bias-flip actions are denoted as $V_0, V_1, \dots, V_M$. In the m^{th} bias-flip action, Figure 6 shows the equivalent circuit and voltage waveform of the transient. The piezoelectric voltage before and after this transient is formulated as follows

$$\gamma\Delta U = \gamma(V_{m-1} - V_{b,m}) = V_m - V_{b,m}. \quad (12)$$

From the equivalent circuit in Figure 6a and the voltage waveform in Figure 6b, the operation of each bias-flip action in SMBF is nearly identical to that in SSHI. The key difference is that voltage flipping in SMBF refers to a bias voltage $V_{b,m}$, instead of zero in SSHI. Given the optimal bias voltage set in (11), it is derived that the voltage steps generated by each bias-flip action have the same magnitude, i.e.,

$$V_{m-1} - V_m = (1 - \gamma)\Delta U, \quad \forall m = 1, 2, \dots, M. \quad (13)$$

The energy absorbed by the m^{th} bias source during a bias-flip action is given by

$$\Delta E_m = (1 - \gamma)C_p\Delta UV_{b,m} \quad (14)$$

A negative value indicates energy delivered by the bias source to the resonant circuit. Given the first characteristic of the optimal bias voltages expressed in the first equation of (11), any bias voltage in the m^{th} bias-flip action, i.e., $V_{b,m}$, can be reused by reconnecting it with reversed polarity to the transient circuit branch in the $(M - m + 1)^{\text{th}}$ round of bias-flip for producing $V_{b,M-m+1}$. Therefore, the net energy gain of the same voltage source after the m^{th} and $(M - m + 1)^{\text{th}}$ rounds of bias-flip actions equals zero.

$$\Delta E_m + \Delta E_{M-m+1} = 0. \quad (15)$$

Equation (15) indicates that, at the optimal condition and steady-state operation, the bias voltage sources are self-sustainable. Therefore, in practical implementation of SMBF circuits, the bias voltage network can be formed by using only a passive capacitor network. No active bias voltage source is needed.

From the original study of SMBF model [19], the harvesting capability of a P-SMBF circuit can be formulated as follows

$$\tilde{R}_{\text{SMBF}} = \frac{M}{\pi} \frac{1 - \gamma}{1 + \gamma} + \frac{1}{\pi}. \quad (16)$$

Here, $\tilde{R}_{\text{SMBF}}$ denotes the dimensionless harvesting capability of the SMBF interface, defined as $\tilde{R}_{\text{SMBF}} = \max_{\tilde{V}_r} [R_h(\tilde{V}_r)] \omega_0 C_p$, where R_h is the equivalent harvesting resistance and the maximum is taken over the normalized rectified voltage $\tilde{V}_r$. Equation (16) includes SEH and P-SSHI as the special cases $M = 0$ and $M = 1$, respectively. Equation (16) shows that the harvesting capability improves as the number of bias-flip actions M increases. However, the harvested power is bounded in practical scenarios, even under excitation with constant displacement magnitude, i.e., ignoring the backward electrical-to-mechanical coupling effect. An increase in piezoelectric voltage leads to more leakage current through the dielectric resistance R_p . This leakage reduces the charge pumped into the bias-flip branch, thus offsetting the rise of v_p . The cancellation effect becomes more pronounced as M increases.

4. Optimal Switched-Capacitor Networks

4.1. Existing Designs

To generate all bias voltage levels from $V_{b,1}$ to $V_{b,M}$, multiple reference voltage sources are required, as illustrated in Figure 5. The bidirectional H-bridge structure enables reuse of $V_{b,m}$ in the m^{th} and $(M - m + 1)^{\text{th}}$ bias-flip operations. Based on this combined reuse mechanism, P-S3BF, the three bias-flip version, can be implemented by using only one flying capacitor [20]. If the voltage across the flying capacitor is V_b , three consecutive bias-voltage levels, V_b , 0, and $-V_b$, can be obtained.

When more than one H-bridge structure is cascaded, extra bias voltages can be produced from the series combination of different bias sources. For example, using two flying capacitors, whose voltages are presumed to be V_b and $2V_b$, we can implement S7BF by realizing seven bias flips via $3V_b$, $2V_b$, V_b , 0, $-V_b$, $-2V_b$, and $-3V_b$, respectively [22].

4.2. Screening Possible Switched-Capacitor Networks

Existing discrete SMBF implementations have achieved up to seven bias-flip actions [22]. The IC counterparts, in particular, the SSHC designs can realize more bias-flip steps [13,18]. However, considering the cost-effectiveness and high-voltage rating requirement of piezoelectric sources, board-level circuits constructed with discrete electronic switching devices are more applicable for immediate and practical PEH applications. It is therefore of interest to maximize the utilization of a limited number of flying capacitors to realize as many bias-flip actions as possible. Limiting the number of capacitors helps reduce the system size and cost.

To maximize the usage of every connected flying capacitor, each capacitor first serves individually as a DC bias source. They can then form as many combinations as possible. These combinations are employed to generate voltages that are consecutive integer multiples of V_b . More series-connected capacitors can generate higher bias voltage. Voltage cancellation (positive and negative in a series branch) and capacitor loop connection should be avoided.

Figure 7 summarizes the candidate switched-capacitor networks considered for one to five flying capacitors. Configurations featuring a loop structure or more than one sub-branch are not considered. After brute-force enumeration, the possible networks are listed in Figure 7. Among all these capacitor networks, the optimal configurations that can generate the maximum flips with a specific number of capacitors are screened and marked in green. Here, “optimal” specifically refers to maximizing the number of consecutive bias-flip actions. This optimization is achieved for a fixed number of flying capacitors. The optimization is subject to the stated topology constraints. It does not imply global optimality in harvested power, efficiency, or circuit complexity.

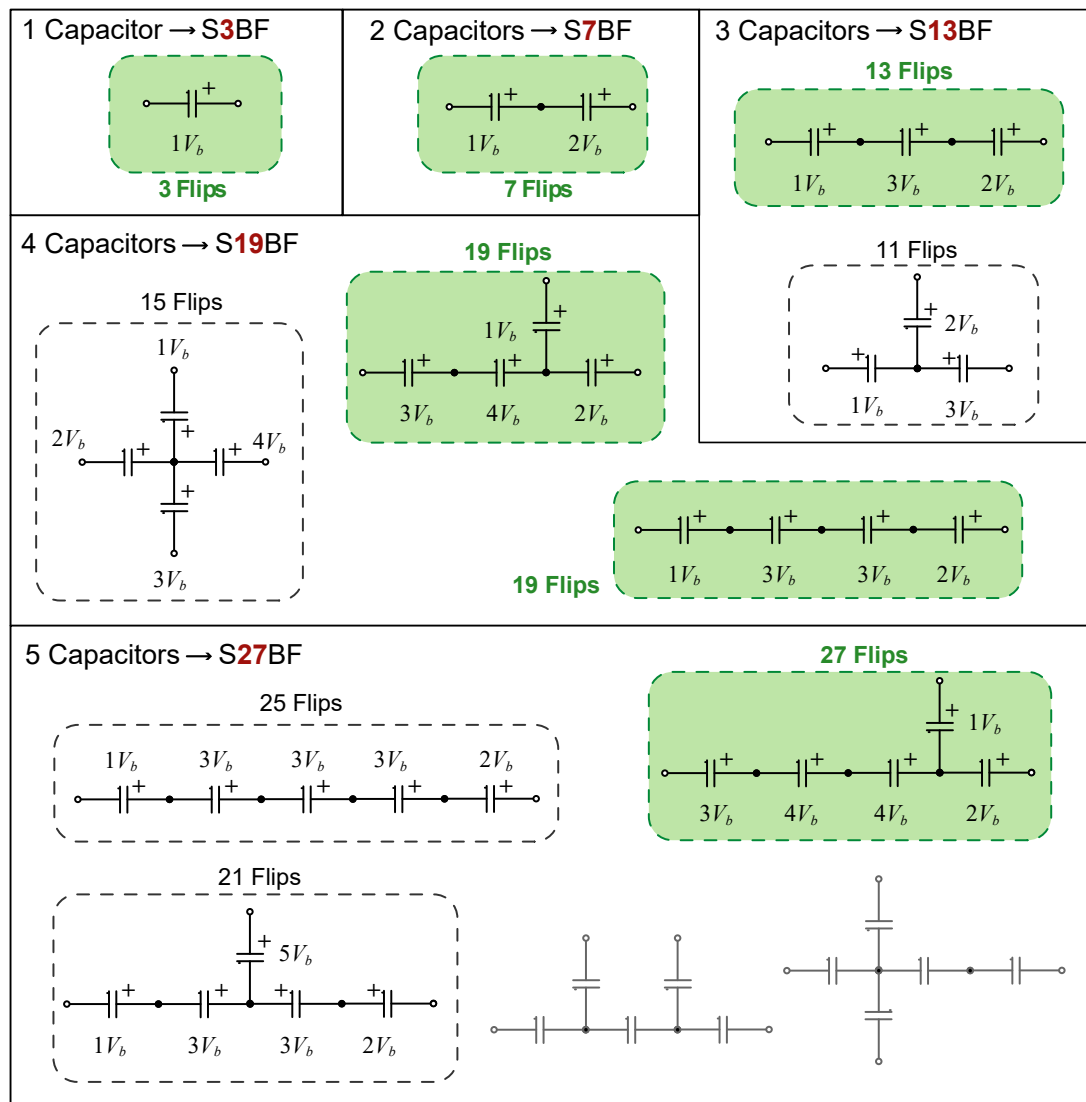


Figure 7. Possible array networks for realizing as many consecutive bias-voltage levels as possible, when utilizing 1–5 flying capacitors. The best options are highlighted in green.

4.3. Switching Network Implementation

The current steering network is derived from the conventional H-bridge topology. An H-bridge structure enables connection of either positive or negative bias voltage to the switching branch. This is accomplished by turning on a diagonal pair of MOSFETs—namely, the low-side transistor on one leg and the high-side transistor on the opposite leg, or the complementary pair. A unidirectional constraint is added to each conducting branch for directing the transient current flow. Since the flying capacitors are connected in series, two adjacent bridges can share one bridge arm.

Figure 8 presents the circuit topologies of P-SMBF for $M = 3, 7, 13, 19$, and 27 . The P-SSH-style energy harvesting circuit comprises a bridge rectifier and a multiple bias-flip branch. The bias-flip branch employs a switched-inductor and switched-capacitor combined network to organize the transient voltage changes. Each current steering unit is formed by four MOSFETs and two diodes. S_{N1} and S_{N2} form a bidirectional switch. S_{N3} and one diode form a unidirectional switch branch that allows current to flow only in the downward direction. S_{N4} and another diode form a unidirectional switch branch that allows current to flow only in the upward direction. Each switch unit is equivalently represented by a red diamond in Figure 8.

Each node of the flying capacitor connects to the midpoint of a switching unit, i.e., V_{CN} . This enables node V_{CN} to be either floating, or connected to V_{b+} , or connected to V_{b-} . By properly driving these switches, the current steering network can reconfigure a capacitor network to produce a series of bias voltages. For example, in the S13BF case, to produce $5V_b$, we can use $V_{C2} - V_{C4}$; to produce $-4V_b$, we can use $V_{C3} - V_{C1}$. The design ensures that the voltage levels from $6V_b, 5V_b, \dots, 0V_b, \dots$, to $-5V_b, -6V_b$ can be realized by taking combinations from the three flying capacitors.

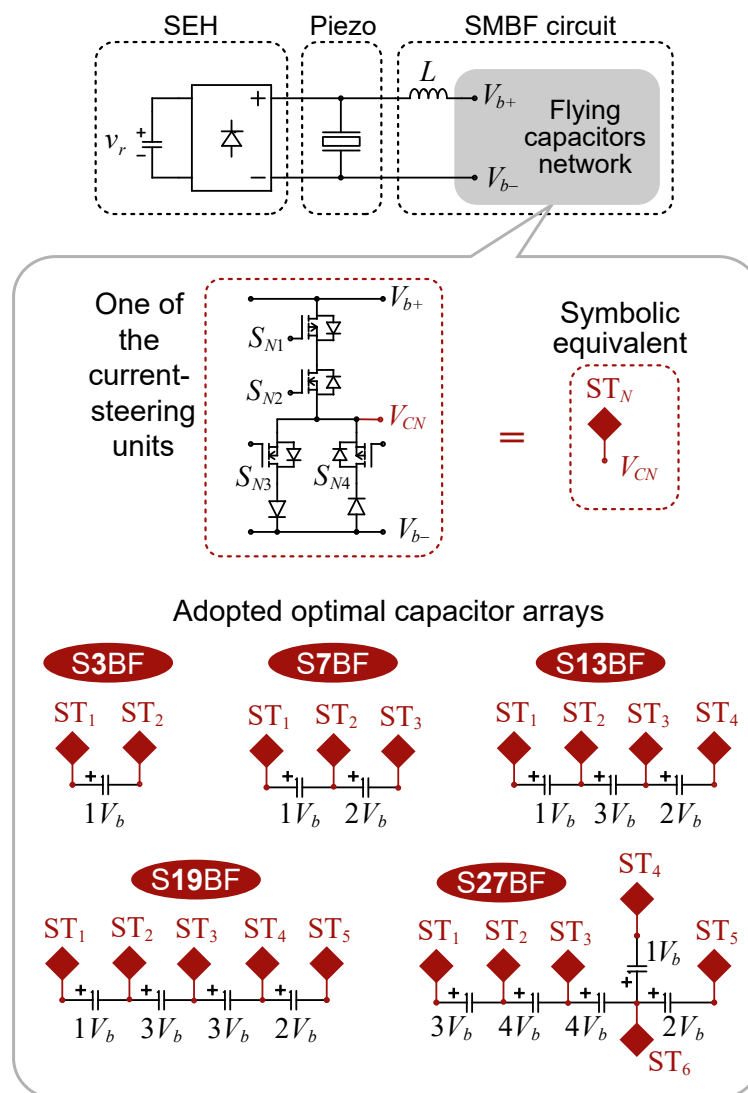


Figure 8. SMBF using the optimal switched-capacitor networks for PEH.

Table 1 shows the two activating units for inserting the corresponding bias voltage in the five optimal SMBF topologies. The connected voltage can be either positive or negative. It depends on the activation of the upper or lower arms in the opposite units.

Table 1. Corresponding switch-on units for realizing all bias voltages in SMBF.

Bias Voltage	1 Fly Cap.	2 Fly Cap.	3 Fly Cap.	4 Fly Cap.	5 Fly Cap.
$0V_b$	ST_1, ST_1	ST_1, ST_1	ST_1, ST_1	ST_1, ST_1	ST_1, ST_1
$\pm 1V_b$	ST_1, ST_2	ST_1, ST_2	ST_1, ST_2	ST_1, ST_2	ST_4, ST_6
$\pm 2V_b$	-	ST_2, ST_3	ST_3, ST_4	ST_4, ST_5	ST_5, ST_6
$\pm 3V_b$	-	ST_1, ST_3	ST_2, ST_3	ST_2, ST_3	ST_1, ST_2
$\pm 4V_b$	-	-	ST_1, ST_3	ST_1, ST_3	ST_2, ST_3
$\pm 5V_b$	-	-	ST_2, ST_4	ST_3, ST_5	ST_3, ST_4
$\pm 6V_b$	-	-	ST_1, ST_4	ST_2, ST_4	ST_3, ST_5
$\pm 7V_b$	-	-	-	ST_1, ST_4	ST_1, ST_3
$\pm 8V_b$	-	-	-	ST_2, ST_5	ST_2, ST_6
$\pm 9V_b$	-	-	-	ST_1, ST_5	ST_2, ST_4
$\pm 10V_b$	-	-	-	-	ST_2, ST_5
$\pm 11V_b$	-	-	-	-	ST_1, ST_6
$\pm 12V_b$	-	-	-	-	ST_1, ST_4
$\pm 13V_b$	-	-	-	-	ST_1, ST_5

4.4. Design Example: S13BF by Using 3 Flying Capacitors

Taking S13BF as an example, the detailed steps for realizing 13 successive bias-flip actions by using 3 flying capacitors are demonstrated in Figure 9. Figure 9a–n show the conducting branches, while Figure 9o shows the $v_p(t)$ waveform. Figure 9 only presents the descending operation. The ascending voltage-flipping operation is symmetric. It utilizes the complementary switches. For other capacitor networks, the working principle is similar. The specific capacitor connections and switching sequences depend on the selected network.

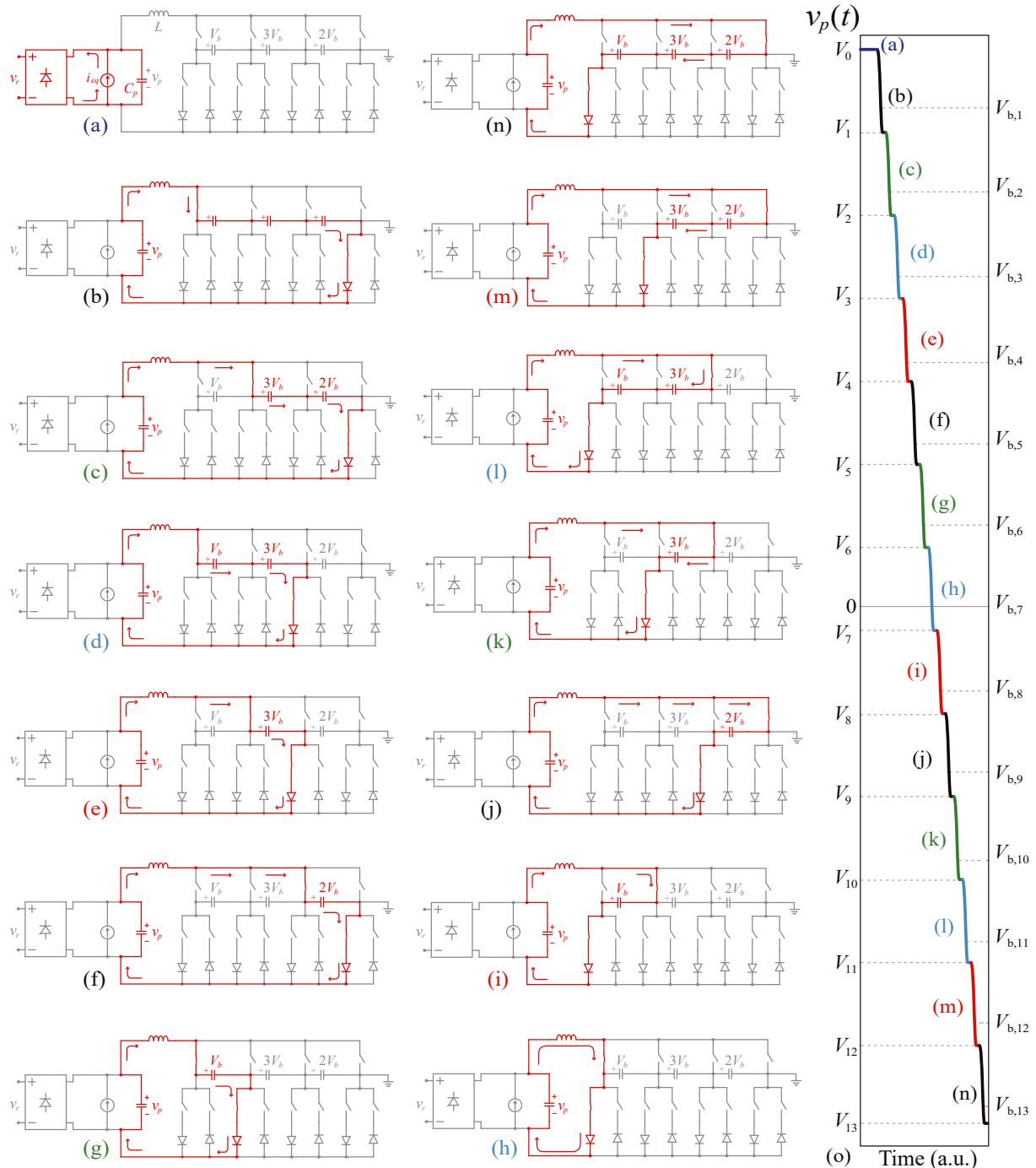


Figure 9. Conducting branches and piezoelectric voltage waveform in S13BF during a positive-to-negative descending voltage flipping transient. (a) Rectifier conduction with the piezoelectric voltage clamped at V_0 . (b)–(n) 13 phases in a flipping transient. (o) Voltage waveform of v_p in a series of descending bias-flip actions.

For simplicity, MOSFET switches are represented as single-pole single-throw (SPST) switches. The output terminal voltage is constant and equals V_0 . All components are assumed ideal, except that the inductor has a limited quality factor. Since the flying capacitors have much larger capacitances than the piezoelectric capacitance, the bias voltage of the connecting source is almost constant in each bias-flip action.

The working phases are summarized as follows

- Charging phase (a): Before the zero-crossing point of i_{eq} , the circuit operates in mode (a). During this phase, the diode bridge conducts and delivers the source current to the load, while the piezoelectric voltage is clamped at V_0 . The bias-flip branches remain deactivated until i_{eq} crosses zero.
- Bias-flip phases (b)–(n): Once i_{eq} crosses zero from positive to negative, 13 bias-flip actions are carried out in sequence. The current steering network steers the current to the capacitor network. C_p , L_i , and the capacitor network form a voltage-inductor-capacitor (VLC) resonant circuit. Since all capacitors in the bias network are significantly larger than C_p , their voltages are treated as constant during the bias-flip operation. With the bias network approximated as a constant-voltage source, the transient can be modeled as a voltage-source-inductor-capacitor circuit. Since C_p is relatively small, the resonant frequency of this VLC circuit is approximately equal to that of the L_i - C_p circuit. The resonant frequency is typically several kilohertz, much higher than that of a typical mechanical structure. Given the rapid reaction of the electrical circuit, i_{eq} is still around 0 after the 13 bias-flip actions.

In mode (b), v_p switches from V_0 to V_1 . The LC resonant loop is biased at $V_{b,1} = 6V_b$. This transient lasts for half of one LC resonant period. When v_p reaches V_1 , the inductor current returns to zero; therefore, potential reverse current is blocked by the steering diode. By blocking reverse current, the steering diode relaxes the MOSFET turn-off timing requirement and avoids the need for active detection of the inductor-current zero crossing during each resonant transition. The next switching configuration must nevertheless be applied only after the preceding transition has finished. In the following operating modes (c) to (g), a series of transient actions further bring v_p down to V_6 . In each action, the flying capacitors slightly gain some amount of energy.

In mode (h), two switches in the same current-steering unit conduct to create a 0-volt bias. v_p is flipped from a positive value V_6 to a negative value V_7 with respect to zero, as it does in P-SSHI.

In mode (i), the capacitor network configuration is identical to that in mode (g). The only difference is reversed polarity to generate $V_{b,8} = -V_b$. Modes (i)–(n) correspond to modes (g)–(b), respectively. These actions further bring v_p down to V_{13} . They adopt the same bias voltages but with reversed polarity. In modes (i)–(n), energy from these bias voltage sources is injected back to C_p . Energy injection, or pre-biasing as referred to in some literature [25], establishes a larger magnitude of v_p to facilitate more energy extraction in the subsequent half vibration cycle. The same amount of energy is input to and output from the same flying-capacitor combination during two symmetric bias-flip operations. This ensures that the bias capacitors maintain energy neutrality.

After mode (n), the circuit enters the open-circuit mode. This mode corresponds to the time interval between t_f and t_c in Figure 3. Under the open-circuit condition, i_{eq} charges C_p in a more negative direction. The charging process continues until v_p reaches $-V_0$. All controlled switches are turned off during the open-circuit mode.

4.5. Bias Voltage Establishment and Adjustment

The final challenge in constructing the switched-capacitor network is establishing and maintaining the proportional voltage values of these flying capacitors. Existing S3BF [21, 26] and S7BF [22] designs have demonstrated self-establishment and self-adjustment capabilities. The single-capacitor S3BF analysis in [20] provides a basic example of the same bias-voltage establishment and adjustment mechanism underlying the higher-order networks, including S27BF, although their coupled capacitor-voltage dynamics are more complex. These topologies can inherently establish and maintain the required proportional voltages without additional control circuits. The only requirement is to properly carry out the designed switching sequence. The flying capacitors can be charged or discharged gradually to the steady-state condition. This convenience is attributed to the two diodes in the current-steering network. These passive switches block one of the symmetric charging or discharging bias-flip actions. Such automatic blocking occurs when the bias voltage requires a transient decrease or rise, respectively, toward a new equilibrium. The transient for bias voltage establishment and adjustment can be shortened by using smaller flying capacitors. However, the performance of smaller capacitors in stabilizing the bias voltage degrades. Thus, selecting a reasonable value of the flying capacitor requires empirical exploration. In general, the value should be more than ten times larger than C_p . This helps provide a stable DC voltage. Meanwhile, the value should not be excessively large. This shortens the transition time from one equilibrium state to another during the establishment and adjustment processes. The present study focuses on steady-state operation; startup settling time, steady-state bias-voltage ripple, and load-transient responses are not quantitatively characterized.

5. Experiments

A circuit prototype is fabricated to validate the feasibility of the larger-M version beyond the reported S3BF and S7BF [22, 26]. The SMBF schemes with different numbers of bias-flip actions are experimentally compared.

5.1. Setup

Figure 10 presents the experimental setup, which consists of a piezoelectric beam driven by a shaker, a printed circuit board (PCB) prototype, and a full-bridge rectifier. The 3D-printed cantilever beam is mounted on a vibration shaker (model: KDJ-20). The piezoelectric patch is connected to the prototype interface circuit. A variable resistor is used to adjust the output load for measuring the harvested power under different loading conditions. A function generator (model: DG1032) produces a sinusoidal driving signal with constant amplitude. A power amplifier amplifies the driving signal and drives the vibration shaker. Given the weak electromechanical coupling, the beam operates under constant displacement magnitude condition. The function generator also provides a square-wave synchronization reference corresponding to the zero crossings of i_{eq} . The ESP32 uses this reference to initiate the programmed bias-flip sequence. Thus, the prototype uses an external synchronization reference rather than an autonomous current zero-crossing detector.

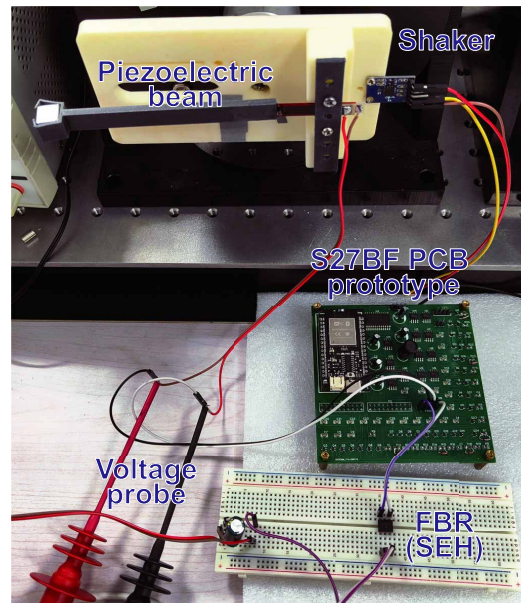


Figure 10. Experimental setup and S27BF PCB prototype.

A microcontroller (model: ESP32) generates the control command sequence for driving MOSFET switches. The PCB prototype supports up to five flying capacitors. It can implement configurations up to S27BF. To compare the performance of different flip counts, only the control sequence needs modification. Table 2 lists the parameters of some key components in the PCB prototype. In the current design, the microcontroller and switch-driving circuit are battery-powered. The harvested power does not account for the power consumption of these auxiliary circuits. Losses in the harvesting path are reflected in the measured output power, but their individual contributions have not been separately quantified. This paper does not emphasize the self-powered feature of the entire circuit design. We investigate the achievable harvesting performance of these sophisticated switching networks. Future work will investigate an ultra-low-power application-specific integrated circuit (ASIC) implementation of the control and gate-driving circuits toward fully self-powered operation.

Table 2. Component parameters in experiment.

Component	Value
Vibration frequency f_0	20.66 Hz
Piezoelectric capacitance C_p	141.6 nF
Inductor L_i	10.06 mH (ESR = 18.4 Ω)
Flying capacitors C_b	4.7 μ F (50 V rating) $\times$ 5 pieces
Filter/storage capacitor C_r	10 μ F
N-channel MOSFET	BSS123W-7-F
P-channel MOSFET	BSS84WQ-7-F
Diode	1N4148WS (5 μ A leakage @75V)
Full bridge rectifier	DB107

5.2. Results

Figure 11 shows the v_p waveform of S27BF in steady-state operation. The 27 successive bias-flip actions collectively reverse the piezoelectric voltage from approximately 5 V to -3.8 V, corresponding to an effective voltage-flipping factor of $\gamma_{\text{eff}} \approx -0.76$, despite the use of a low- Q inductor. In steady state, the bias voltages of five flying capacitors are measured with a multimeter. They are measured to be 0.96 V, 1.19 V, 1.23 V, 0.64 V, and 0.31 V, respectively. Taking 0.31 V as V_b , the voltage ratio is calculated as 3.10 : 3.84 : 3.97 : 2.06 : 1, which is close to the designed theoretical value of 3 : 4 : 4 : 2 : 1. Only the representative S27BF waveform is shown in this paper. The other SMBF schemes can be implemented by changing the control sequences. All realized bias voltages and their ratios are measured and listed in Table 3. These measurements confirm that the flying-capacitor bias voltages approach the intended ratios during steady-state operation.

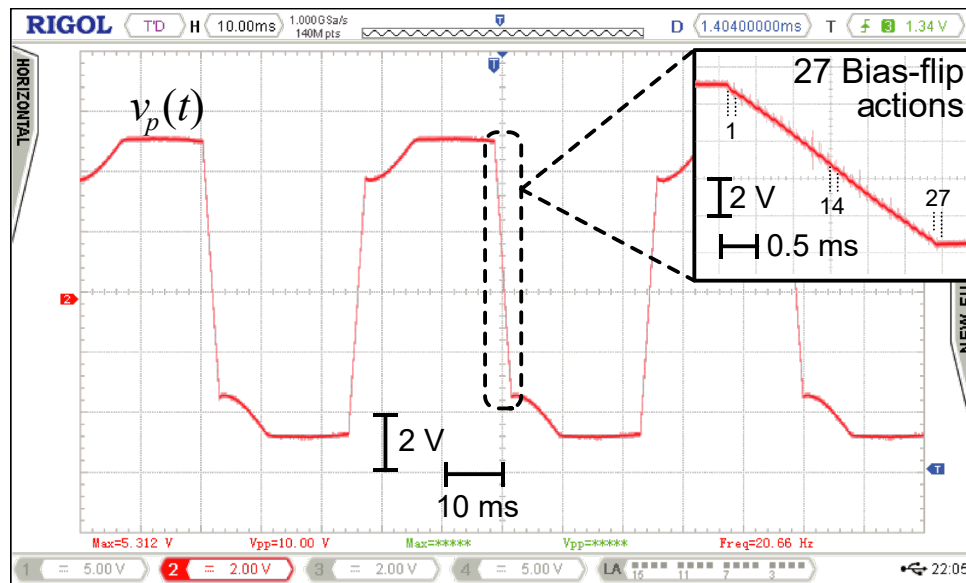


Figure 11. Piezoelectric voltage v_p waveform for the $M = 27$ case, i.e., S27BF, under a 200 k Ω load.

Table 3. Measured bias voltages in steady-state operation and their practical and ideal ratios.

M	Absolute Bias Voltage (V)	Relative Ratio (xV_b)	Theoretical Ratio (xV_b)
1	0	-	-
3	2.05	1	1
7	2.08, 1.03	2.02 : 1	2 : 1
13	1.17, 1.8, 0.61	1.92 : 2.95 : 1	2 : 3 : 1
19	0.89, 1.23, 1.3, 0.44	2.02 : 2.80 : 2.95 : 1	2 : 3 : 3 : 1
27	0.96, 1.19, 1.23, 0.64, 0.31	3.10 : 3.84 : 3.97 : 2.06 : 1	3 : 4 : 4 : 2 : 1

Figure 12 summarizes the harvested power of different SMBF schemes under the same steady-state harmonic vibration. The SEH case can be regarded as a special case with $M = 0$, i.e., without any bias-flip action, while P-SSHI corresponds to the S1BF case with a single bias-flip action. As the flip number M increases, the harvested power also increases. Using the measured SEH peak power as the reference, the ratios of the peak harvested powers are given by

$$P_{h,\text{max,SEH}} : P_{h,\text{max,P-SSHI}} : P_{h,\text{max,P-S3BF}} : P_{h,\text{max,P-S7BF}} : P_{h,\text{max,P-S13BF}} : P_{h,\text{max,P-S19BF}} : P_{h,\text{max,P-S27BF}} \\ = 1.0 : 2.11 : 2.74 : 3.25 : 3.62 : 3.70 : 3.89. \quad (17)$$

It shows that a larger M , i.e., more bias-flip actions, leads to a larger peak harvested power in the SMBF solutions. Practical nonidealities, including dielectric loss, diode forward-voltage drops, and losses in the switching network, limit the achievable power enhancement. Two relevant limitations are discussed below. First, the ideal SMBF theory fails to fully account for the dielectric loss of practical piezoelectric materials. Only the harvested power boosting capability is considered from the perspective of switched-capacitor circuit design. Dielectric loss can significantly degrade the power boosting effect during bias-flip operations [27]. Second, the effect of voltage

drop of practical diodes is not fully considered in the ideal SMBF model. As M increases, each bias-flip voltage step approaches the diode voltage drop. The fixed diode voltage drop hinders the further enhancement of v_p magnitude.

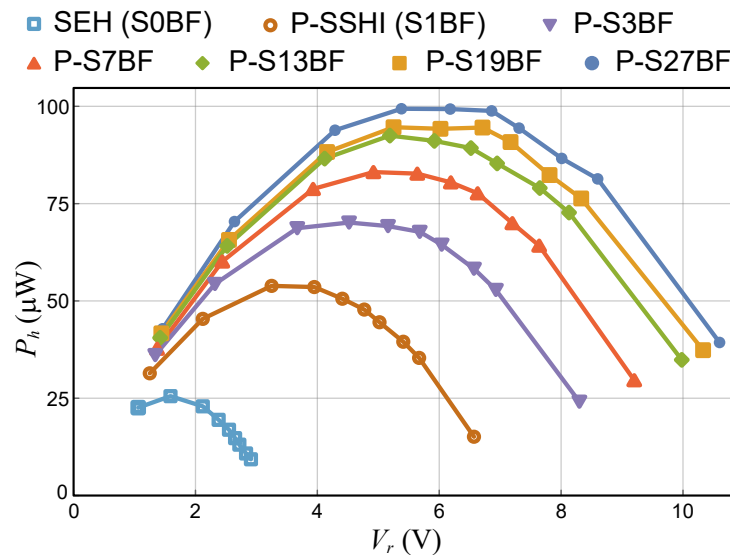


Figure 12. Harvested power under different rectified voltages (corresponding to different loading conditions) and numbers of bias-flip actions M . Open-circuit voltage $V_{oc} = 7.82$ V in all cases.

6. Conclusions

With the advancement of power electronics, boosting harvested power via synchronized bias-flip actions in piezoelectric energy harvesting has been studied over the past two decades. This paper investigates the optimal switched-capacitor network to maximize the utilization of a limited number of flying capacitors. By adopting this reconfigurable network, the S19BF with 19 bias-flip actions can be implemented using only four flying capacitors. The S27BF with 27 bias-flip actions can be achieved with five flying capacitors. To the best of our knowledge, this work demonstrates the highest number of experimentally verified bias-flip actions among discrete-component PEH interfaces reported to date. Experiments validate the S27BF circuit and confirm the performance improvement of the SMBF approach. The experiments demonstrate increased harvested power with increasing M , while practical circuit nonidealities limit the incremental improvement. Therefore, future research should explore trade-offs between performance enhancement, implementation complexity, and application requirements.

7. Biographies of the Authors



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Author Contributions

J.Q.: conceptualization, methodology, investigation, visualization, and writing original draft preparation; L.C.: experiment, measurement, visualization, and writing review; J.L.: supervision, validation, project administration, funding acquisition, and writing review and editing. All authors have read and agreed to the published version of the manuscript.

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The authors declare no conflict of interest.

Use of AI and AI-Assisted Technologies

During the preparation of this work, the authors utilized ChatGPT for language editing. After using this tool, the authors reviewed and edited the content as necessary. The authors take full responsibility for the content of the published article.

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