

Extending Conversion Ratio of a Series-Capacitor Buck Topology by Adding N Capacitor Cells

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Abstract: This paper introduces an extension methodology for modular multi-phase series-capacitor buck converter that enables scaling to an arbitrary number of capacitor cells, with minimum operation states and minimum topological subcircuits. By distributing the voltage conversion across multiple capacitive stages, the new design reduces device voltage stress and improves overall efficiency. The converter extension using a basic capacitor cell enables a highly modular architecture with a minimal component count and distinguished subcircuits while supporting high conversion ratios. The interaction between the capacitor and the inductor results in a soft charging operation, which reduces the losses of the converter, and contributes to higher efficiency. Additional features of the new converter include a significantly extended effective duty ratio, reduced inductor and output current ripple, high output current capability, and architecture-inherent output current sharing that balances the loading between the phases. Simulation and experimental results obtained from a modular, interleaved-two-phase, three-capacitor-cell prototype validate the developed methodology and demonstrate strong agreement with the theoretical analyses.

Keywords: data center; DC-DC power converters; high conversion ratio; point-of-load converter; series capacitor buck converter; voltage regulator module

1. Introduction

The increasing demand for high-performance power delivery in data centers and telecommunication systems has driven the development of converters with higher efficiency, greater current and power density, and larger conversion ratios [1–4]. The increased popularity of using a 48 V DC power distribution network in today's computing industry has reinforced the need for DC–DC point of load (PoL) systems capable of carrying the conversion of 48 V-to-1.x V [5,6]. Hybrid converters have recently attracted considerable attention in high conversion ratio, low-voltage, high-frequency DC-DC applications [7–11]. By combining capacitive and inductive switching networks, these topologies reduce component stress, size, and switching losses while maintaining or improving efficiency. Among various designs, two stand out for their potential: the multi-level flying capacitor (MLFC) buck converter [12,13] and the series-capacitor buck (SCB) converter [14–18].

MLFC converters have been widely adopted in high power applications [19]. This type of converter lowers the switching node voltage without adding more phases and ensures equal voltage stress across all switches under steady state. However, it faces two main challenges: the need for active balancing of flying capacitor voltages and the presence of many synchronous rectification (SR) switches [20,21]. In high-ratio conversions, the converter operates in the SR state for a significant portion of the time. Consequently, the SR switches must be large to minimize the conduction losses, and their size increases with the number of levels.



The traditional SCB, being inherently multi-phase, naturally balances currents between phases and passively stabilizes its flying capacitor voltages. It has only one SR switch per phase but requires at least one switch rated for the full input voltage. Lowering the switching node voltage in the SCB is achieved by adding more phases and therefore more components. For example, a two-phase SCB uses two inductors, four switches, and achieves a $V_{in}/2$ switching node voltage swing, whereas reducing the voltage swing to $V_{in}/3$ requires three phases, three inductors, and six switches [22–24], and so forth for higher numbers of phases. Numerous SCB derivatives reported in the literature combine the Dickson switched-capacitor topology with a dual-inductor buck converter. These topologies reduce the switch stress by employing multiple capacitors, switches, and subcircuits [25–28], where there is no specific attention devoted to minimizing the number of subcircuit states, and as a result larger number of components is required.

The objective and the novelty of this study is to introduce an extension methodology for modular multi-phase series-capacitor buck converter to an arbitrary number of capacitor cells, with minimum operation states and minimum topological subcircuits.

This work builds on the SCB concept and introduces to it N capacitor cells connected in series (Figure 1). The unique operation mode that minimizes the number of states and subcircuits in the resulting converter reduces energy losses and component count. In addition, these modifications allow significant reduction in the switching nodes voltage swing, higher voltage conversion ratio, reducing the output ripple without adding more inductors or phases, and utilizing a single SR switch in each conduction path (switches S_{1L} and S_{2L} shown in Figure 1). The topology depicted in Figure 1, is implemented with three capacitor cells and two inductors. It effectively quadruples the duty ratio, lowers the transistors' voltage stress and features natural current sharing between the phases. The modular stacking of generic capacitor cells contributes to great flexibility in the design, enables high-conversion ratio, and suits 48 V-to-1.x V single-stage converter solution.

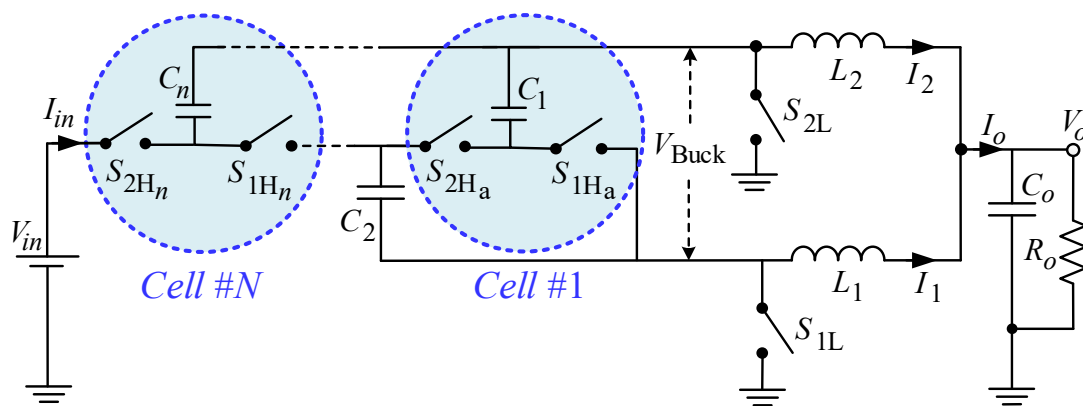


Figure 1. SCB topology constructed with N capacitor cells.

2. Modular Series Capacitor Buck

The development of the capacitor cell as a fundamental building block is illustrated in Figure 2. The cell includes a capacitor and a pair of complementary switches and multiple cells can be connected in series. Throughout this study, the concept is presented and analyzed using a configuration of three capacitor cells and two inductors, as illustrated in Figure 1. The capacitor cells are connected according to a simple procedure, where port “a” of the cell (Figure 2) is connected to the next cell (or to V_{in} in the case of the last cell); port “b” of the cell is connected either to the lower or upper inductor, L_1 or L_2 respectively; and port “c” is connected to the previous cell (or to the lower inductor L_1 , in the case of the first cell). When two cells are combined, one common series switch (S_{1H}), as illustrated in Figure 2, could be omitted without disrupting the functionality of either cell.

The operation of the three-capacitor SCB topology is described using the ideal timing diagram in Figure 3 and the subcircuits in Figure 4, with highlighted current paths. The same timing diagram of Figure 3 is applicable to any number of capacitor cells. The switching period is divided into four intervals, corresponding to four operating states (I–IV). As in conventional multiphase converters, all phases deliver a continuous current to the output through an interleaved buck-type connection. Since the charging and discharging of the capacitors occur through an inductance, the charge transfer is referred to as soft charging [29,30].

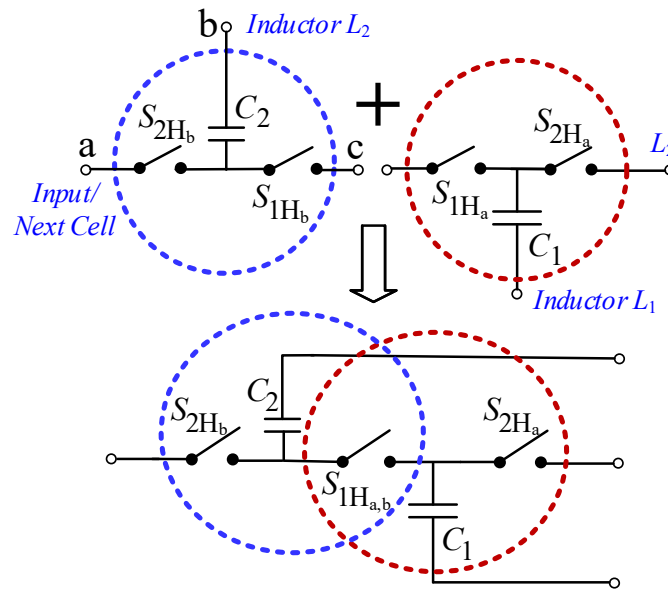


Figure 2. Combination of two capacitor cells.

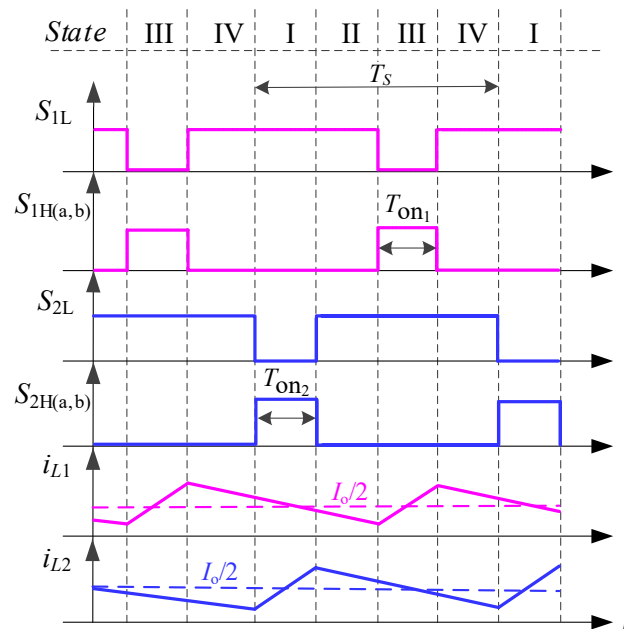


Figure 3. Timing diagram and idealized waveforms of a two phase SCB converter.

State I (Figure 4a) is the charging state for phase 2, while phase 1 discharges to the load. Switches S_{2Ha} , S_{2Hb} and S_{1L} are turned ON and capacitor C_3 and inductor L_2 are charged from the input while simultaneously delivering current to the load. Inductor L_1 continues to supply current to the load. Capacitor C_1 is charged from C_2 and C_2 is discharged to the load. The average voltage relationship between the input source and the three capacitors is summarized as follows:

$$V_{in} - V_{C3} = V_{C2} - V_{C1} \quad (1)$$

States II and IV (Figure 4b) are balancing states in which neither phase is charged. Switches S_{1L} and S_{2L} are ON, and both inductors deliver current to the load. All capacitor voltages remain unchanged. In addition to balancing functionality, this state introduces time separation interval between switches that otherwise would potentially experience a shoot-through, such as $S_{1H(a,b)}$ and $S_{2H(a,b)}$.

State III (Figure 4c) is the charging state for phase 1, while phase 2 discharges to the load. Switches S_{2L} and S_{1H} are ON, and inductor L_1 is charged from two parallel sources: capacitor C_1 and a series connection of C_3 and C_2 (where C_3 is connected in a positive direction and C_2 is connected in a negative direction). As a result of this configuration, C_3 transfers charge to capacitor C_2 , and the average voltage relationship between the three capacitors is as follows:

$$V_{C3} - V_{C2} = V_{C1} \cdot \quad (2)$$

During this state, inductors L_1 and L_2 continue to deliver current to the load. All states operate in soft-charging mode. In this paper, a “cell” refers to an individual building block (i.e., a capacitor cell), whereas a “phase” refers to an electrical phase characterized by its corresponding inductor current.

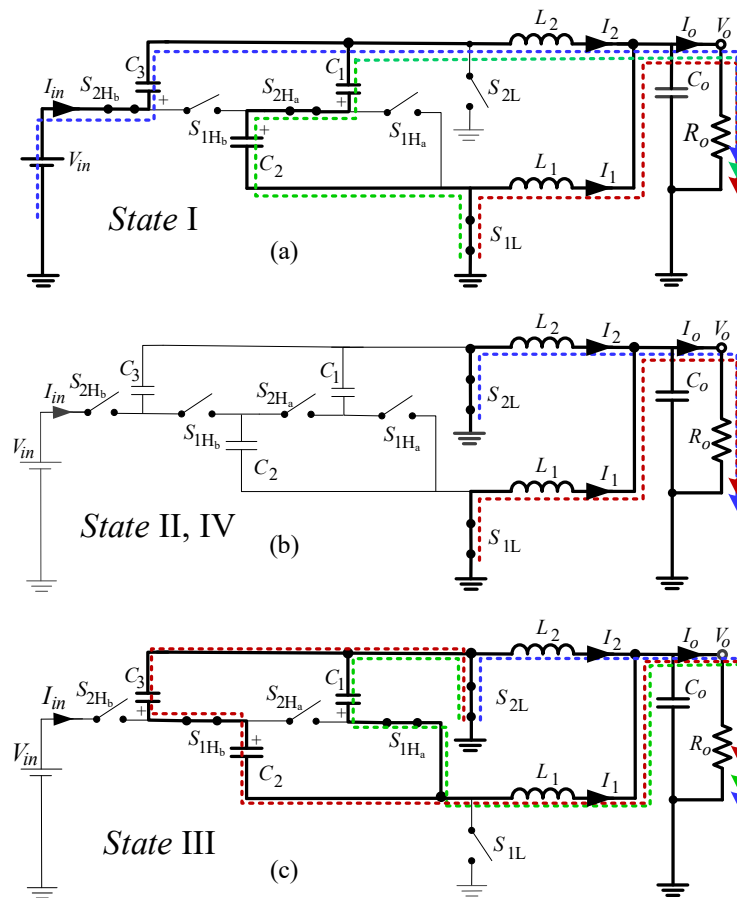


Figure 4. SCB with a three-capacitor-cells implementation. Operation states I-IV. (a) State I: phase 1 is OFF, and phase 2 is ON. (b) States II and IV: both phases are OFF. (c) States III: phase 1 is ON, phase 2 is OFF.

3. Steady-State Analysis

For simplicity, the following analysis assumes that the voltage ripple across all capacitors is negligible compared to their DC levels.

3.1. Conversion Ratio

The current ripple of inductors L_1 , and L_2 during “on” and “off” intervals can be expressed as follows:

$$\Delta i_{L1} = \left| \frac{(V_{C1} - V_o)}{L_1} \right| D_1 T_s = \left| \frac{V_o}{L_1} \right| (1 - D_1) T_s, \quad \Delta i_{L2} = \left| \frac{(V_{in} - V_{C3}) - V_o}{L_2} \right| D_2 T_s = \left| \frac{V_o}{L_2} \right| (1 - D_2) T_s, \quad (3)$$

where $D_1 = T_{on1}/T_s$ and $D_2 = T_{on2}/T_s$. Inductor L_1 is discharged during states I, II, and IV and charged during state III. Inductor L_2 is discharged during states II, III and IV, and charged during state I.

Without loss of generality, and assuming equal inductance values, the following voltage relationship can be derived from (3):

$$\begin{cases} V_o = D_1 V_{C1} \\ V_o = D_2 (V_{in} - V_{C3}) \end{cases}, \quad (4)$$

Using Equations (1) and (2), and solving (4) for the average capacitors’ voltages, yields the following:

$$V_{C1} = \frac{D_2}{2(D_1+D_2)} V_{in}; V_{C2} = \frac{D_1+D_2}{2(D_1+D_2)} V_{in}; V_{C3} = \frac{D_1+2D_2}{2(D_1+D_2)} V_{in}. \quad (5)$$

Combining (4) and (5), converter voltage gain can be expressed as follows:

$$M = \frac{V_o}{V_{in}} = 1 / \left(\frac{2}{D_1} + \frac{2}{D_2} \right) = \frac{D_1 D_2}{2(D_1 + D_2)}. \quad (6)$$

For the particular case of equal duty ratios in the two phases, $D_1 = D_2 = D$, the average capacitor voltages converge to $V_{C1} = V_{in}/4$, $V_{C2} = 2 V_{in}/4$, and $V_{C3} = 3 V_{in}/4$. and the expression for the converter voltage gain reduces to:

$$M = \frac{V_o}{V_{in}} = \frac{D}{4}. \quad (7)$$

The effect of series-capacitor stacking can be analyzed using (7), which indicates that the conversion ratio of the new topology is four times higher than that of a typical buck converter.

For the general case of N capacitor cells connected in series, assuming an equal duty cycle is applied to all phases, the conversion ratio can be expressed as follows:

$$M = \frac{V_o}{V_{in}} = \frac{D}{N+1}. \quad (8)$$

Average capacitor voltages per cell can be expressed as follows:

$$V_{Cn} = n \left(\frac{1}{N+1} \right), \quad (9)$$

where n is the capacitor index, ranging from 1 to N .

3.2. Inductor Currents

The average inductor currents for each phase expressed in terms of output current for the case of odd number of cells N and equal duty cycles applied to all phases is summarized as $I_{L1} = I_{L2} = I_o/2$. In the case of even number of cells N , the average inductor currents are expressed as follows:

$$I_{L1} = \frac{N+2}{2N+2} I_o, \quad I_{L2} = \frac{N}{2N+2} I_o. \quad (10)$$

The ratio between the average inductor currents in the case of even number of cells, using (10), takes the form of (11):

$$\frac{I_{L1}}{I_{L2}} = 1 + \frac{2}{N}. \quad (11)$$

The normalized inductor currents, I_{L1}/I_o and I_{L2}/I_o , derived from (10), are shown in Figure 5. For the case of even N , increasing the number of capacitor cells improves the current symmetry between the inductors approaching the ultimate balance $I_{L1,2}/I_o = 1/2$.

Assuming an equal duty ratio, $D_1 = D_2 = D$, the inductors current ripple in the case of $N = 3$ cells can be derived from (3) and (5) as:

$$\Delta i_{L1} = \frac{(V_{in}/4 - V_o)D}{L_1 f_s}, \quad \Delta i_{L2} = \frac{(V_{in}/4 - V_o)D}{L_2 f_s}. \quad (12)$$

The inductor current ripple in the generic case of N capacitor cells, takes the form of (13):

$$\Delta I_{L1} = \frac{(V_{in}/(N+1) - V_o)D}{L_1 f_s}, \quad \Delta I_{L2} = \frac{(V_{in}/(N+1) - V_o)D}{L_2 f_s} \quad (13)$$

It can be observed from (13) that higher number of capacitor cells contributes to the reduction of the inductors current ripple.

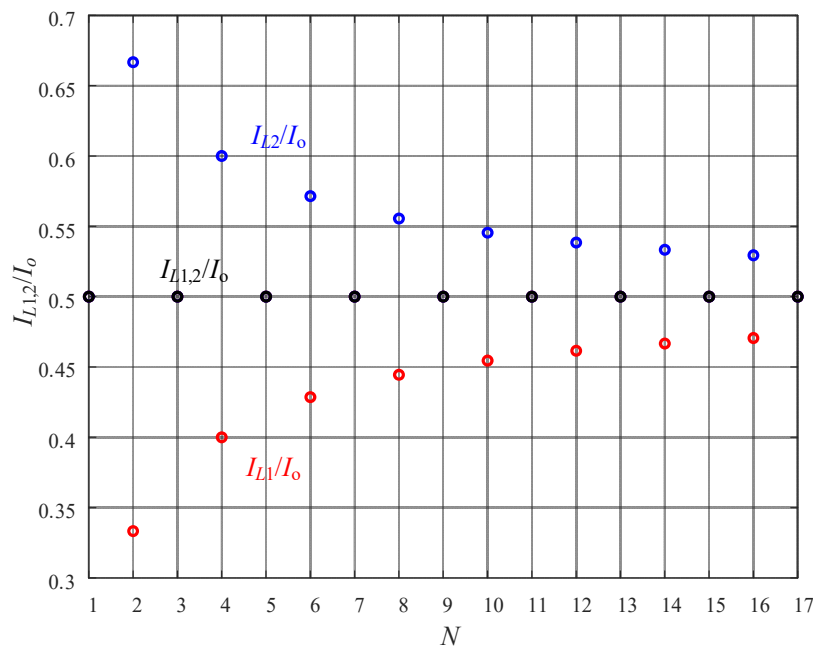


Figure 5. Normalized inductor currents, I_{L1}/I_o and I_{L2}/I_o .

3.3. Soft Charge/Discharge

The condition for soft charging is the presence of a current-carrying inductance in the charge and discharge paths of the flying capacitors [29]. Hard charging occurs when two capacitor branches are directly connected in parallel. In the case of imperfect symmetry between the capacitor voltages in the circuit, state III (Figure 4c) may experience hard switching for some short periods upon state changes. There, high current spikes may arise as a result of voltage mismatch between branches ($C_2 + C_3$ in parallel to C_1). In this case, behavior similar to soft charging of the flying capacitors can be achieved by operating in partial-charge mode [30]. When the switching time is much shorter than the time constant of the flying-capacitor loop circuit, the current is practically constant during the switching state time and hence the RMS current reaches its minimum value. This condition can be expressed as follows:

$$T_j \ll R_j C_j, \quad (14)$$

where R_j is the total ESR and C_j is the total capacitance of the corresponding loop in each switching state, and T_j is the duration of the associated time interval.

Applying a generic capacitor cell structure in the schematic and in the physical layout are some of the measures to remedy this issue as it significantly reduces voltage mismatches due to parasitic elements. The use of low ESR capacitors is recommended to further reduce the potential voltage mismatch as a result of component uncertainties, when paralleling capacitors.

3.4. Stress on Switches

The expression for the maximum voltage stress across each converter switch during all operating states is summarized in Table 1, with an example for a 48 V-to-1 V application presented in the rightmost column. The low-side switches S_{1L} and S_{2L} , as well as the high-side switch S_{2Hb} , experience a relatively low voltage stress of $(1/4) V_{in}$. The high-side switches S_{1Ha} , S_{2Ha} , and S_{1Hb} are subjected to higher stress levels of $(1/2) V_{out}$ during one of the switching states. These maximum voltage-stress values represent the highest possible voltage that may appear across each switch in any switching stage. The presence of flying capacitors is the key factor in reducing the voltage stress across each of the MOSFETs, and this stress can be further reduced by increasing the number of cells in the converter.

For higher-order converters, the general expression for maximum switch voltage stress as a function of V_{in} , relative to converter order, is summarized in (15) and an example for up to eight cells is shown in Table 2.

$$S_{1,2L} (n \geq 1) = \frac{V_{in}}{(n+1)}, \quad S_{nH(a,b)} (n > 1) = \frac{2V_{in}}{(n+1)}. \quad (15)$$

A higher converter order results in a lower voltage stress on both low-side and high-side switches for a similar voltage conversion ratio. It is worth noting that the SR switches ($S_{1,2L}$) conduct for much longer periods of time and, as a result, carry a much higher average current during the discharge states. They are exposed to half the voltage stress compared to the high-side switches, making it possible to select a lower resistance switch to further reduce conduction losses. The absolute value of V_{Buck} (as shown in Figure 1) represents the maximum stress on the SR switches and can be expressed as $V_{\text{Buck}} = V_{\text{in}}/(N+1)$.

The SCB converter with N capacitor cells employs a total of $N+3$ switches. N of these switches are subjected to a maximum voltage stress of $2 V_{\text{in}}/(N+1)$, whereas the remaining three switches experience a reduced voltage stress of $V_{\text{in}}/(N+1)$.

Table 1. Switches voltages of each state in the three-capacitor-cell converter.

Switch	State				Stress *
	I	II	III	IV	V_{max} [V]
S_{1L}	0	0	V_{C1}	0	12
S_{2L}	$V_{\text{in}}-V_{C3}$	0	0	0	12
S_{1Ha}	V_{C2}	$V_{C2}-V_{C1}$	0	$V_{C2}-V_{C1}$	24
S_{2Ha}	0	$V_{C2}-V_{C1}$	$V_{C3}-V_{C1}$	$V_{C2}-V_{C1}$	24
S_{1Hb}	$V_{C3}-V_{C1}$	$V_{C3}-V_{C2}$	0	$V_{C3}-V_{C2}$	24
S_{2Hb}	0	$V_{\text{in}}-V_{C3}$	$V_{\text{in}}-V_{C3}$	$V_{\text{in}}-V_{C3}$	12

The blue shade indicates the highest stress per switch. * $V_{\text{in}} = 48$ V, $M = 1/48$.

Table 2. An example of maximum switch voltage vs. the number of capacitor cells in a converter.

# Cap Cells	2	3	4	5	6	7	8
Switch							
$S_{1,2L} (N \geq 1)$ *	$(1/3) V_{\text{in}}$	$(1/4) V_{\text{in}}$	$(1/5) V_{\text{in}}$	$(1/6) V_{\text{in}}$	$(1/7) V_{\text{in}}$	$(1/8) V_{\text{in}}$	$(1/9) V_{\text{in}}$
$S_{nH(a,b)} (N > 1)$	$(2/3) V_{\text{in}}$	$(2/4) V_{\text{in}}$	$(2/5) V_{\text{in}}$	$(2/6) V_{\text{in}}$	$(2/7) V_{\text{in}}$	$(2/8) V_{\text{in}}$	$(2/9) V_{\text{in}}$

* Includes S_{2Hb} .

3.5. CCM-DCM Boundary

The inductor current valley can be summarized as follows:

$$I_{L1,2(\min)} = I_{L1,2(\text{Av})} - \frac{\Delta i_{L1,2}}{2}, \quad (16)$$

where $I_{L1,2(\min)}$ is the valley, $I_{L1,2(\text{Av})}$ is the average, and $\Delta i_{L1,2}$ is the peak-to-peak ripple of the inductor current. For a converter operation in continuous conduction mode (CCM), the inductor current must always remain positive. Setting $I_{L1,2(\min)}$ to zero in (16) yields the CCM–DCM boundary condition [31–33]. Assuming equal duty cycles, the average inductor currents for odd number of cells are $I_{L1} = I_o/2$ and $I_{L2} = I_o/2$. In the general case, using (10), (13), and (16), the inductor current valley for the case of odd and even N can be summarized as follows:

$$I_{L1,2(\min)} = \underbrace{\frac{I_o}{2}}_{I_{L1,2(\text{Av})}} - \underbrace{\frac{(V_{\text{in}}/(N+1)-V_o)D}{2L_{1,2}f_s}}_{\Delta i_{L1}/2}, \quad (17)$$

for odd N , and

$$I_{L1(\min)} = \underbrace{\frac{N}{2N+2} I_o}_{I_{L1(\text{Av})}} - \underbrace{\frac{(V_{\text{in}}/(N+1)-V_o)D}{2L_1 f_s}}_{\Delta i_{L1}/2}, \quad I_{L2(\min)} = \underbrace{\frac{N+2}{2N+2} I_o}_{I_{L2(\text{Av})}} - \underbrace{\frac{(V_{\text{in}}/(N+1)-V_o)D}{2L_2 f_s}}_{\Delta i_{L2}/2}, \quad (18)$$

for even N .

The CCM–DCM boundary for the case of odd N is represented in (19):

$$L_{1,2\min} = \frac{DR_o}{f_s} \left(\frac{1}{M(N+1)} - 1 \right). \quad (19)$$

The CCM–DCM boundary for the case of even N is represented in (20):

$$L_{1\min} = \frac{DR_o}{f_s} \left(\frac{1-M(N+1)}{M(N+2)} \right), \quad L_{2\min} = \frac{DR_o}{f_s} \left(\frac{1-M(N+1)}{NM} \right). \quad (20)$$

3.6. Power Losses

The power-stage losses in a DC–DC converter are classified into two major categories: conduction losses and switching losses. In this study, power loss is analyzed using the three-capacitor-cell topology as a representative example. For simplicity it is assumed that the duty ratios for both phases are equal, i.e., $D_1 = D_2 = D$.

Conduction losses are evaluated under CCM, assuming sufficiently small current ripple such that the average current approximates the RMS current.

The series capacitor power conduction loss is given by:

$$P_{\text{Series_Cap}} = I_{C_{\text{RMS}}}^2 R_{\text{ESR}}, \quad (21)$$

where the ESR is the equivalent series resistor of the capacitor.

The RMS currents of the capacitors can be calculated based on the fact that all three flying capacitors operate in soft charging and discharging mode [29,30]. In this mode capacitor current waveform is well approximated by a trapezoidal shape. The absolute value of all capacitor currents pulses is equal and matches the input current pulse, both in value and shape. Therefore, the capacitor currents can be directly derived from the input current. The energy stored in C_3 during State I by the input current is transferred to C_2 during State III. This energy is subsequently transferred from C_2 to C_1 during State I, as demonstrated by the circuit operation analysis presented in Section 2.

Assuming current ripple is negligibly small compared to the current peak of the pulse, the trapezoidal pulse waveform can be further approximated as a rectangular pulsating waveform. Consequently, the RMS value of the input current, assuming a single pulse per switching period (State I), can be expressed as a function of its average value as follows:

$$I_{\text{in(RMS)}} = \frac{I_{\text{in(Avg)}}}{\sqrt{D}}, \quad (22)$$

where the average input current can be expressed as a function of the conversion ratio M as follows:

$$I_{\text{in(Avg)}} = \frac{D}{4} I_{\text{out(Avg)}}. \quad (23)$$

Following these relations, the RMS capacitor current can be calculated as follows:

$$I_{C(\text{RMS})} = \frac{|I_C|_{\text{Avg}}}{\sqrt{2D}} = \frac{2I_{\text{in(Avg)}}}{\sqrt{2D}}. \quad (24)$$

The inductor conduction loss can be expressed as:

$$P_L = I_{L(\text{Avg})}^2 R_{\text{DCR}}, \quad (25)$$

where R_{DCR} is the DC parasitic inductor resistance.

For example, in the three-capacitor-cell topology, the power losses of inductors L_1 and L_2 can be expressed by considering the average inductor currents as follows:

$$P_{L_1} = \left(\frac{1}{2} I_{\text{out}} \right)^2 R_{\text{DCR}}; \quad P_{L_2} = \left(\frac{1}{2} I_{\text{out}} \right)^2 R_{\text{DCR}} \quad (26)$$

The conduction loss in the MOSFETs can be calculated by considering the average current in each state and the parasitic resistance $R_{DS(on)}$, which can be expressed as:

$$P_{\text{MOSFET}} = I_{DS}^2 \cdot R_{DS(on)} \cdot (\Delta t_{\text{State}} / T_s), \quad (27)$$

where Δt_{State} denotes the MOSFET conduction time associated with a specific state or a combination of states. For example, the power loss for the low side switches, S_{1L} during states 1, 2, 4 and S_{2L} , during states 2, 3, 4 can be summarized as follows:

$$P_{S_{1L}} = I_{L1 \text{ (St. 1,2,4)}}^2 R_{DS(on)} (1-D) + \left(\frac{1}{2} I_{L2 \text{ (St. 1)}} \right)^2 R_{DS(on)} D = \left(\frac{1}{2} I_{out} \right)^2 R_{DS(on)} (1-D) + \left(\frac{1}{4} I_{out} \right)^2 R_{DS(on)} D = \left(\frac{4-3D}{16} \right) I_{out}^2 R_{DS(on)} \quad (28)$$

$$P_{S_{2L}} = I_{L2 \text{ (St. 2,3,4)}}^2 R_{DS(on)} (1-D) + I_{L1 \text{ (St. 3)}}^2 R_{DS(on)} D = \left(\frac{1}{2} I_{out} \right)^2 R_{DS(on)} (1-D) + \left(\frac{1}{2} I_{out} \right)^2 R_{DS(on)} D = \left(\frac{1}{2} I_{out} \right)^2 R_{DS(on)} \quad (29)$$

The power loss for high side switches, S_{1H} , S_{2H} and S_{1-2} , can be calculated using (30)–(33):

$$P_{S_{1Ha}} = I_{C1(RMS) \text{ _State 3}}^2 R_{DS(on)} D = I_{in(RMS)}^2 R_{DS(on)} \quad (30)$$

$$P_{S_{1Hb}} = I_{C3(RMS) \text{ _State 3}}^2 R_{DS(on)} D = I_{in(RMS)}^2 R_{DS(on)} \quad (31)$$

$$P_{S_{2Ha}} = I_{C2(RMS) \text{ _State 1}}^2 R_{DS(on)} D = I_{in(RMS)}^2 R_{DS(on)} \quad (32)$$

$$P_{S_{2Hb}} = I_{in(RMS)}^2 R_{DS(on)} \quad (33)$$

where the switches currents are derived from the input and capacitor currents.

Switching losses are defined as the overlap between the voltage and current of the MOSFET during the “on” to “off” transition and are calculated as follows [34]:

$$P_{SW} = \frac{1}{6} \cdot V_{DS_{max}} \cdot I_{D_{max}} \cdot (t_r + t_f) \cdot f_s \quad (34)$$

where V_{DS} is the drain-to-source voltage, I_D is the drain current, and t_r and t_f are the rise and fall times, respectively.

The total power loss of the three-capacitor-cell topology is therefore expressed as:

$$P_{Loss(T)} = P_{C(T)} + P_{L(T)} + P_{MOSFET(T)} + P_{SW(T)} \quad (35)$$

where $P_{Loss(T)}$, $P_{SW(T)}$, $P_{MOSFET(T)}$, $P_{L(T)}$, $P_{C(T)}$ represent the total loss in a converter, switching losses, and MOSFET losses respectively.

4. Simulation and Experimental Results

Steady-state simulation waveforms for a 50 W, 48 V-to-1 V converter operating at a 333 kHz switching frequency per phase, and delivering an output current of 50 A with equal duty ratios, are shown in Figure 6. The simulation compares three SCB implementations with different numbers of capacitor cells, i.e., $N = 1, 2$, and 3 . The simulation shown in Figure 6a demonstrates the output voltage, inductor currents in CCM, output currents, and V_{Buck} . Figure 6b demonstrates the capacitor voltage and the SR switches voltages for different numbers of capacitor cells, i.e., $N = 1, 2$, and 3 . As can be seen from Figure 6, increasing the number of capacitor cells reduces the stress on the switching devices, while maintaining CCM operation.

To validate the operation of the SCB topology with three flying capacitors at a high voltage and high conversion ratio, a 100 W laboratory prototype operating at a switching frequency of 333 kHz per phase was built and tested. The component values and nominal parameters of the experimental prototype are summarized in Table 3. Each phase of the converter was designed to be identical, as can be seen in the photograph of the experimental prototype (Figures 6b and 7a). Each capacitor cell consists of a flying capacitor formed by three 10 μ F capacitors connected in parallel to reduce the ESR, and a dual N -Channel MOSFET. A microchip dsPIC33 controller is used to generate complementary gate waveforms for switches S_{nL} and S_{nH} . Figure 8 presents the measured inductor currents and output current waveforms at $M = 1/48$. The measured capacitor voltages are $V_{C1} = 11.82$ V, $V_{C2} = 23.7$ V, and $V_{C3} = 35.7$ V, as shown in Figure 9. The measured power-stage efficiency is shown in Figure 10. Three output voltages of 1.0 V, 1.2 V, and 1.5 V are demonstrated operating at a constant input voltage of 48 V.

To validate the equations presented in Subsection 3.6, the power-loss breakdown is calculated for the power stage of the three-capacitor-cells converter using component parameters listed in Table 3. The analysis is performed for operation point of $I_{out} = 40$ A, $V_{out} = 1$ V, which is the maximum efficiency point of the converter.

The analysis includes the switching losses of the MOSFETs, the conduction losses of the inductors, flying capacitors, and high side and low side MOSFETs (Figure 11). The calculated peak efficiency at $V_{out} = 1$ V and 40 W is 95.73%, whereas the measured efficiency is 94.55%. The calculated peak efficiency at $V_{out} = 1.5$ V and 60 W is 97.2%, whereas the measured efficiency is 96.4%. These differences are mainly attributed to the temperature-dependent drift of the component parasitic parameters and the inductor core losses, which were not taken into account in the calculated loss breakdown. As shown in Figure 11, the SR conduction losses are the main contributors to the overall power loss.

A comparative performance review of state-of-the-art single-stage wide conversion ratio solutions and the SCB comprised of three capacitor cells presented in this study is summarized in Table 4.

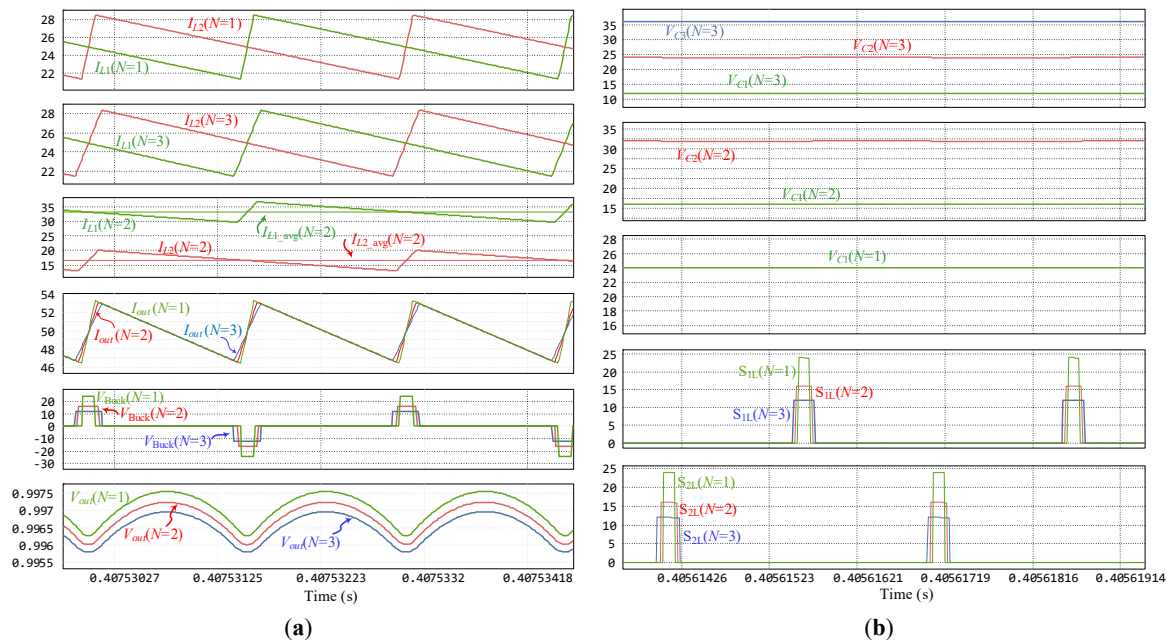


Figure 6. Simulation results of the SCB converter with different numbers of capacitor cells, for $M = 1/48$: (a) inductor currents, output current, V_{Buck} , and output voltage for $N = 1, 2$, and 3; (b) capacitor voltage and SR switch voltage for $N = 1, 2$, and 3. The Y-axis units are volts [V] for voltage measurements and in amperes [A] for current measurements.

Table 3. Experimental Prototype Parameters.

		Power Stage
Component	P/N	Value/Type
Input voltage— V_{in}		48 V
Output voltage— V_{out}		1–1.5 V
Switching freq.— f_s		333 kHz per phase.
Input capacitor— C_{in}	EEE-FK2A221AV	220 μ F, 100 V
Output capacitor— C_{out}	EEF-GX0D561R	560 μ F, 2 V
Inductors— L_1, L_2, L_3	XAL1580_401MEB	0.4 μ H, 60 A, DCR = 0.5 m Ω
Capacitors— C_1, C_2, C_3	C5750X7S2A106M	10 μ F, 100 V, ESR = 4 m Ω
MOSFETs	NVMFD5C446NL	$R_{DS\ on}$ = 2.2 m Ω , 145 A
Load resistance— R_{load}		10–100 m Ω
Floating Driver		
Driver	2EDF7275F	
Isolated DC/DC	TDR 3-1212SM	
Digital Section		
Microcontroller	dsPIC33FJ16GS502	16 bit, 40 MIPS
Buffers and drivers	MC74VHC244DWR2G	

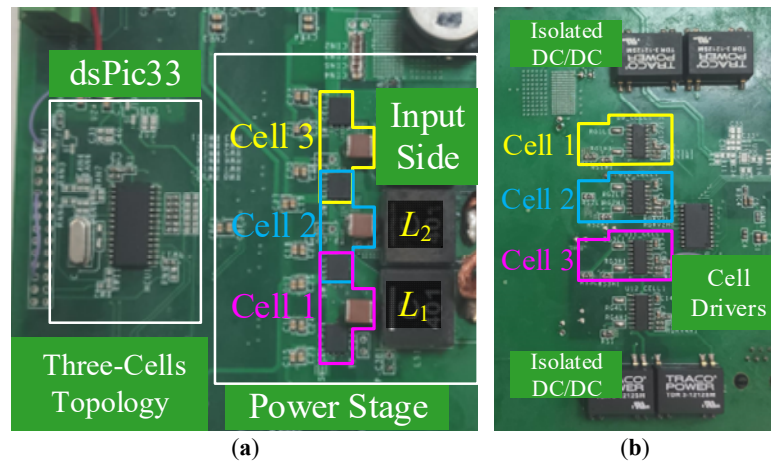


Figure 7. Prototype PCB: (a) top view of the power stage, including the microcontroller, dual *N*-Channel MOSFETs per cell, flying capacitors, and power inductors; (b) bottom view, including a buffer, drivers, and isolated DC–DC supplies.

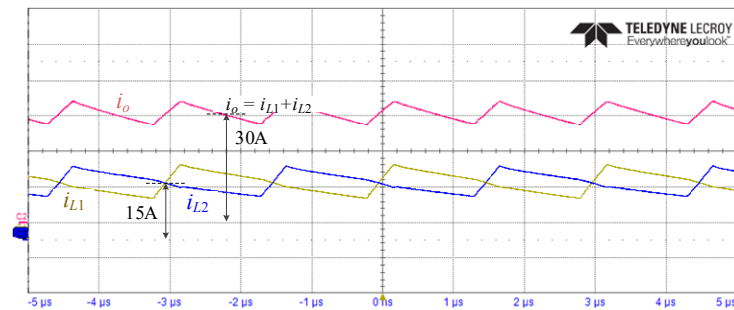


Figure 8. Experimental inductor and output current waveforms ripple and phase shift: yellow– i_{L1} , blue– i_{L2} , pink–output current. The phases are interleaved by 180 degrees and output ripple frequency is twice the switching frequency. Horizontal scale: 1 μ s/div. Vertical scale: 10 A/div.

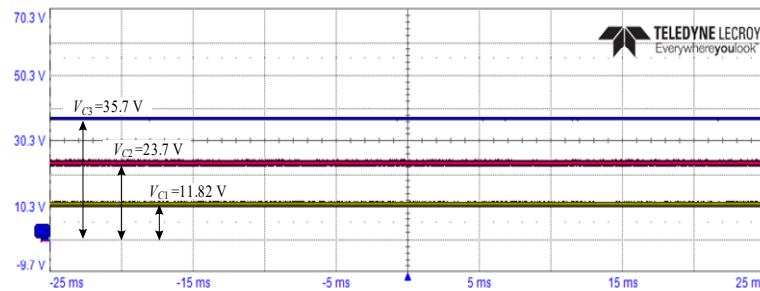


Figure 9. Experimental results at $M = 1/48$, $V_{out} = 1$ V and $P_{out} = 50$ W. C_1 , C_2 and C_3 , series capacitors voltages 10 V/div, Horizontal scale: 5 ms/div.

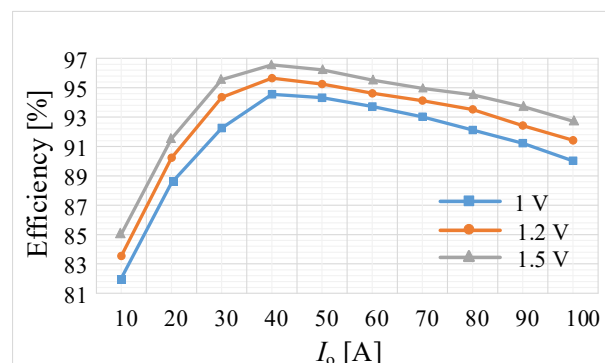


Figure 10. Experimental efficiency results measured at different output voltages.

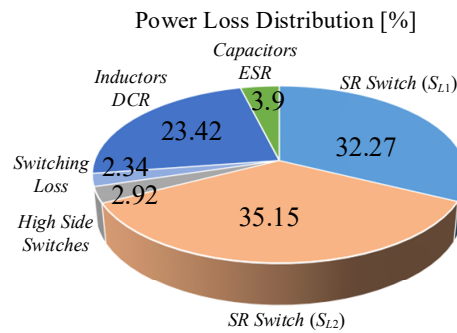


Figure 11. Power loss breakdown calculation of the three-capacitor-cells topology for experimental prototype operated under the conditions of: $M = 1/48$, $V_{out} = 1$ V, $P_{out} = 40$ W and $f_s = 333$ kHz.

Table 4. A performance review of state-of-the-art single stage wide conversion ratio solution (power stage).

Topology/Reference	Extended SCB (This Work)	DIH [25]	SDIH [26]	TLAHD [27]	DPHD [28]
M (Generalized Form)	$D/(N+1)$	D/N	D/N	$D/2N$	Even: $2D/[(N+2)D + (N-2)]$, Odd: $2D/[(N+1)D + (N-1)]$
Tested Ratio	$D/4$	$D/6$	$D/6$	$D/12$	$D/(4D+3)$
Tested Range	48 V to 1–1.5 V /100 A	48 V to 1–2 V/10 A	48 V to 1–3 V /46 A	48 to 0.6–1.5 V/30 A	48 to 1–2 V/30 A
#Switches	6	8	10	11	10
#Flying Capacitors	3	5	10	6	6
#Inductors	2	2	2	2	1
#Diodes	--	2	--	--	--
Switch Stress *	$3 \times (1/4) V_{in}$, $3 \times (2/4) V_{in}$	$5 \times (1/6) V_{in}$	$10 \times (1/6) V_{in}$	$5 \times (1/6) V_{in}$, $4 \times (1/12) V_{in}$, $2 \times (1/2) V_{in}$	$2 \times (2 V_{in} - 8 V_o)/6$, $5 \times 2(V_{in} - V_o)/6$, $3 \times V_o$
Capacitor Stress *	$(3V_{in}/4)$, $(V_{in}/2)$, $(V_{in}/4)$	$(5V_{in}/6)$, $(4V_{in}/6)$, $(3V_{in}/6)$, $(2V_{in}/6)$, $(1V_{in}/6)$	$2 \times \{(5V_{in}/6)$, $(4V_{in}/6)$, $(3V_{in}/6)$, $(2V_{in}/6)$, $(1V_{in}/6)\}$	$(6V_{in}/12)$, $(5V_{in}/12)$, $(4V_{in}/12)$, $(3V_{in}/12)$, $(2V_{in}/12)$, $(1V_{in}/12)$	$(2V_{in} + 4V_o/3)$, $(2V_{in} + V_o/3)$, $(V_{in} + 5V_o/3)$, $(V_{in} + 2V_o/3)$, $2V_o$, V_o
Peak Efficiency ** [%] (Power Stage)	96.5 (1.5 V/40 A), 94.2 (1 V/38 A)	95.02 (2 V, 5.5 A)	89.8 (3 V/33 A), 88.2 (2 V/26 A), 83.5 (1 V/38 A)	91.77 (1 V, 13 A)	92.7 (2 V, 15 A), 90.6 (1 V, 13 A)
Switching Frequency	333 kHz	300 kHz	750 kHz	500 kHz	250 kHz
#Subcircuits/States	4	6	6	8	4

* The stress on the capacitors and switches is quantified as the product of number of components and their respective voltage stress. ** For comparison purposes, the maximum efficiency reported in each manuscript is listed in Table 4. It should be noted that these values may not have been obtained under identical operating conditions.

5. Conclusions

An extension methodology for a modular series-capacitor buck topology based on N series-connected capacitor cells has been presented. The stacking approach enables flexible design with a minimal number of components and subcircuits while achieving high conversion ratios without compromising efficiency. The modular structure provides scalability and preserves inherent phase current sharing. Soft-charging operation is maintained across all operating states and flying-capacitor paths, improving efficiency. For non-ideal conditions resorting to partial-charge operation prevents efficiency drop. These features enable a compact and efficient solution for high step-down-ratio applications, particularly for direct 48-V-to-1.x-V conversion in data center power delivery systems.

A comprehensive steady-state analysis of the N -cell topology is developed, including conversion ratio, capacitor voltage distribution, inductor current ripple, CCM–DCM boundary conditions, switch voltage stress, and power-loss mechanisms. The analysis shows that odd values of N provide better symmetry in the average inductor currents, and as a result have the same CCM–DCM boundary. Increasing the number of capacitor cells by adding one capacitor and one switch significantly increases the conversion ratio, reduces switch voltage stress, and contributes to lower inductor current ripple. Furthermore, the N capacitor-cells topology operates with only four subcircuits regardless of the number of capacitor cells. The power-loss breakdown indicates that the two SR switches account for the largest portion of the total converter losses (approximately 60–70%), whereas the high-side switches and capacitor ESR contribute the least (approximately 3–4%). The theoretical analysis is experimentally validated using a two-phase interleaved prototype with three capacitor cells. Experimentally obtained data demonstrate good agreement with theoretical predictions and simulation results.

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Prof. Peretz has authored more than 200 scientific publications and holds over 30 patents, with a significant portion of the technologies licensed and knowledge transferred worldwide. He served as an advisory board member and tech mentor for a variety of industries worldwide. In 2019, together with two of his PhD graduates, Prof. Peretz founded CaPow Ltd., a breakthrough startup enhancing productivity through Power-in-Motion, where he currently serves as the Chief Executive Officer.

Author Contributions

E.H.: conceptualization, methodology, software and hardware, validation, data curation, formal analysis, investigation, writing—original draft preparation, writing—review and editing, visualization; M.E.: investigation, formal analysis, writing—original draft preparation, writing—review and editing; M.M.P.: supervision, conceptualization, methodology, investigation, formal analysis, writing—original draft preparation, writing—review and editing. All authors have read and agreed to the published version of this manuscript.

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Conflicts of Interest

The authors declare no conflict of interest.

Use of AI and AI-Assisted Technologies

No AI tools were utilized for this paper.

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