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Review

Battery Equalization Systems: A Systematic Review of Topologies, Architectures, and Application Scenarios

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How To Cite: Wei, Z.; Chung, H.S.-H. Battery Equalization Systems: A Systematic Review of Topologies, Architectures, and Application Scenarios. *Power Electronics Research and Applications Transactions* **2026**, *1*(1), 3.

Received: 13 June 2026
Revised: 29 July 2026
Accepted: 4 August 2026
Published: 10 August 2026

Abstract: The large-scale deployment of electric vehicles and grid battery energy storage systems has made cell inconsistency a primary constraint restricting pack capacity utilization, cycle life, and operational safety. Most existing reviews on battery equalization focus on circuit topology analysis, placing less emphasis on architecture evaluation and unified benchmarks, which makes performance comparison and industrial scheme selection challenging. This paper presents a systematic review of battery equalization systems, structured along five interconnected dimensions: application-specific requirements, hardware topologies, energy routing architectures, standardized performance metrics, and the impact of electrochemical characteristics on equalization. Specifically, this work quantifies the diverse design requirements across transportation, grid storage, and aerospace applications, and evaluates the scalability evolution from passive to active topologies. Furthermore, this work establishes a capacity-independent benchmarking framework. This framework adopts path-dependent system efficiency and concurrent throughput as core metrics, and enables objective performance evaluation of various energy routing architectures. Ultimately, the inherent boundaries of voltage-based equalization are clarified by quantifying the correlation between open-circuit voltage versus state-of-charge (OCV-SOC) characteristics and equalization difficulty. By mapping the technological transition from isolated circuit-level optimization to macroscopic energy routing, this review establishes a definitive roadmap for engineering highly scalable and autonomous battery management systems.

Keywords: active equalization; battery equalizer; battery management system; energy storage systems; lithium-ion batteries

1. Introduction

Driven by the global decarbonization transition, battery energy storage systems and electric vehicles have become core components of modern power and transportation infrastructure [1,2]. To meet high voltage and power demands, lithium-ion cells are assembled into large-scale series–parallel packs [3]. Nevertheless, cell inconsistency, induced by manufacturing deviations, inhomogeneous thermal distribution, and nonlinear aging effects, remains a bottleneck in practical applications [4]. This discrepancy triggers the "barrel effect", where the overall performance of the entire pack is constrained by the weakest cell, significantly curtailing usable capacity and increasing the risk of catastrophic thermal runaway [5]. Figure 1 illustrates the state-of-charge (SOC) distribution of 95 retired series-connected battery cells. When the cell with the lowest SOC (green bar) reaches full discharge, the entire pack can no longer output energy. Conversely, when the cell with the highest SOC (orange bar)

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reaches full charge, the pack cannot continue charging. This directly demonstrates that the usable energy capacity of the entire battery pack is strictly limited by SOC inconsistency.

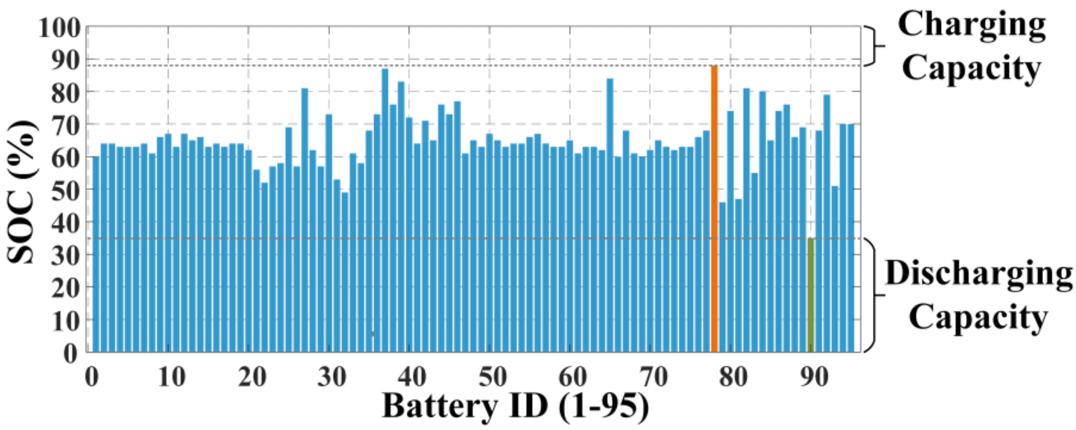

Figure 1. Empirical SOC distribution of a 95-cell retired battery string [6–8].

The battery equalization system serves as a critical functional part within the battery management system (BMS), tasked with dynamically redistributing energy to maintain cell uniformity [9]. Effective equalization is no longer merely a performance enhancement but a fundamental requirement for ensuring the operational safety and economic viability of battery packs [10].

Battery equalization systems have developed over decades, transitioning from passive energy dissipation to active charge redistribution [11]. Early research focused on topological design, using inductor-, capacitor-, and transformer-based structures to implement energy transfer between cells [12,13]. However, as battery packs grow to hundreds of cells, optimizing individual converter circuits cannot improve performance. The macroscopic energy routing path, rather than single circuit efficiency, has become another factor affecting equalization performance. Therefore, the research focus has shifted from circuit topology optimization to architectural-level energy pathway design, evolving from spatially constrained adjacent cell-to-cell structures to position-decoupled distributed modular architectures [14,15].

Although many studies have proposed new equalization structures, many optimizations may not perfectly align with the needs of practical applications. Therefore, this paper outlines the requirements of battery equalization systems for battery energy storage systems in different application scenarios. In addition, existing performance comparisons in literature contain ambiguities. Different studies adopt inconsistent test benchmarks, cell chemistries, and SOC operating ranges, which makes objective cross-comparison of equalization speed and energy efficiency difficult. This absence of standardized metrics not only prevents fair assessment of emerging topologies, but also brings great uncertainty to solution selection in practical industrial applications. Establishing a unified evaluation methodology is critical for the engineering deployment of equalization technologies.

The main contributions of this work are summarized as follows.

(1) This paper systematically quantifies the differentiated equalization performance requirements across transportation, grid storage, second-life battery and aerospace application scenarios.
(2) This work comprehensively reviews and compares equalization topologies based on different energy storage intermediates and macroscopic energy routing architectures, identifying the advantages and applicable scenarios of each scheme.
(3) A capacity-independent performance evaluation methodology is proposed to eliminate the ambiguity caused by inconsistent test conditions in existing literature.
(4) The fundamental correlation between open-circuit voltage versus state-of-charge (OCV-SOC) characteristics and equalization difficulty is quantified, providing a theoretical basis for matching equalization architectures to specific cell chemistries.

The remainder of this paper is organized as follows. Section II quantifies the specific equalization requirements across diverse application scenarios. Section III reviews the evolution of hardware topologies. Section IV systematically compares macroscopic energy routing architectures. Section V establishes the capacity-independent performance evaluation methodology. Section VI analyzes the impact of device OCV-SOC characteristics on challenges in equalization. Finally, Section VII concludes the paper.

2. Application Scenarios and Demand Analysis

As illustrated in Figure 2, battery systems, including both stationary battery energy storage systems (BESS) and on-board electric vehicle packs, serve as the core energy buffer across a wide range of applications, from grid-scale renewable integration to transportation and specialized aerospace missions [16–20]. Despite the huge differences in operating scale and environmental constraints across these fields, they all face the same core hardware challenge: parameter inconsistency among cells in the string [21–23].

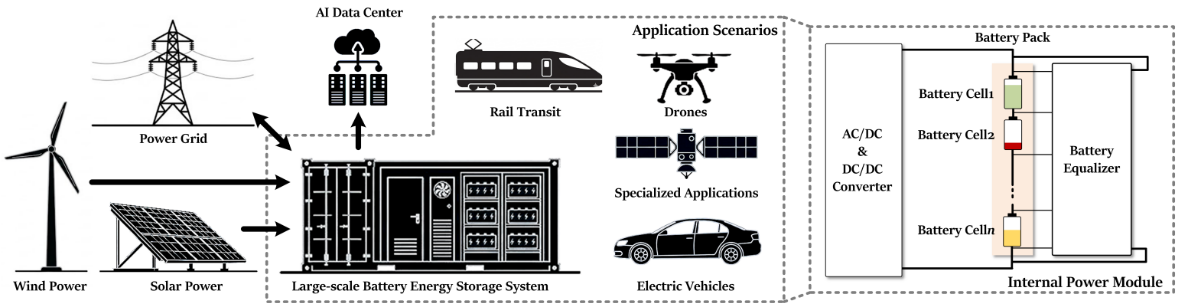

Figure 2. System-level integration of BESS across diverse application domains and the detailed hardware configuration of an internal battery power module with an integrated equalization system.

2.1. Transportation

Transportation represents the primary application field for battery equalization technology, spanning EVs, micro-mobility devices, unmanned aerial vehicles (UAVs), and rail transit systems. These platforms impose strict performance requirements on battery packs regarding driving range, operational safety, cycle life, and dynamic response [24–26].

2.1.1. Passenger Electric Vehicles (EV/HEV/PHEV)

Electric vehicles (EVs), hybrid electric vehicles (HEVs), and plug-in hybrid electric vehicles (PHEVs) are the largest application field for battery equalization technology [27]. The core objective of equalization in this scenario is to maximize driving range and extend pack cycle life by ensuring uniform cell utilization [28].

Electric vehicle battery packs operate under highly dynamic load conditions, with high-rate current pulses during acceleration and regenerative braking [29]. Under such transient states, the substantial Ohmic voltage drop across the internal resistance, coupled with severe polarization effects, significantly distorts the cell terminal voltage. Consequently, conventional control strategies relying solely on terminal voltage differences are highly susceptible to false equalization, where energy is erroneously transferred from a cell with a lower SOC to one with a higher SOC. Therefore, advanced equalizers require fast response and robust state-estimation to maintain true equalization accuracy during dynamic operation [30,31]. In addition, vehicle integration imposes strict space and weight constraints, which requires equalization hardware to achieve high power density with minimal heat generation [32]. Passive equalization is still widely used in low-cost applications due to its simple structure and high reliability. However, its inherent energy dissipation and heat generation characteristics directly conflict with the low thermal and high power density requirements of modern high-capacity EV packs, rendering it unsuitable for ultra-fast charging and long-range vehicle applications [33]. Therefore, the industry is gradually shifting to active equalization architectures to reduce heat generation and enable more flexible energy management [34]. The core challenge of active equalization for EVs is the trade-off between increased component count and system reliability. For large EV packs with hundreds of cells, advanced routing architectures must deliver significant efficiency improvements and support functional integration (such as synchronous state diagnosis) to justify the added hardware complexity [35].

2.1.2. Micro-Mobility

Micro-mobility platforms including electric two-wheelers, e-bikes and scooters serve an extremely cost-sensitive market. In contrast to passenger electric vehicles, which typically have less cost constraints for battery management systems, micro-mobility applications demand highly cost-effective equalization solutions [36]. Design priorities are minimal component count and high silicon integration to cut manufacturing costs [37]. As a result, these applications mostly use simplified passive equalization circuits or highly integrated single-chip active solutions, which trade off high current capability for small size and low unit cost [38].

2.1.3. Unmanned Aerial Vehicles (UAVs)

The core design constraint for UAV equalization systems is the strict trade-off between equalization capability and structural weight/volume [39], so specific power (power-to-weight ratio) is the primary design priority. Therefore, equalization topologies based on transformers or large inductors require a large number of magnetic components, which bring excessive weight and volume, making them less suitable for UAV applications. Meanwhile, UAV battery packs typically have a low series cell count and low operating voltage, rendering them well suited for equalization solutions based on low-voltage semiconductor devices. Consequently, the architectural design for UAV equalizers has minimal requirements for system scalability and modularity. Unlike large-scale energy storage systems, the limited number of cells in UAV packs allows the use of highly centralized, non-modular architectures without notable global efficiency degradation. Similar to electric vehicle batteries, UAV batteries are also affected by dynamic load transients, and operate at higher C-rates during aggressive flight maneuvers [40]. These high discharge rates significantly increase ohmic voltage drop and polarization effects compared to EV applications. As a result, equalization strategies based solely on terminal voltage measurements will introduce noticeable false equalization errors [41].

2.1.4. Rail Transit and Special Vehicles

The high power demand of rail transit operations requires hybrid energy storage systems (HESS). As shown in the Ragone plot in Figure 3, rail systems typically use a hybrid architecture combining fuel cells, supercapacitors and lithium-ion batteries to balance system energy and power requirements [42].

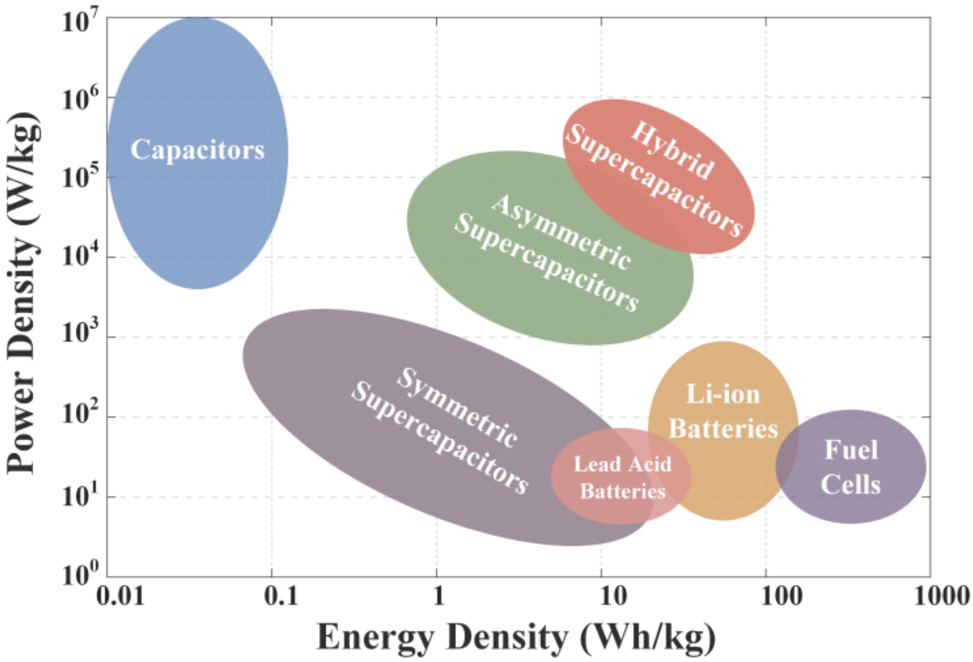

Figure 3. Ragone plot comparing the energy and power densities of various state-of-art supercapacitors and batteries [43,44].

Compared to consumer electronics and passenger EVs, heavy-duty rail platforms have completely different equalization design requirements. Unlike consumer devices that prioritize low cost and small size, rail systems are designed for 20 to 30 years of continuous operation, requiring strict compliance with railway lifecycle and safety standards such as EN 50126[45]. Most importantly, rail battery packs operate at very high voltage levels, typically 750 V to over 1500 V, so equalization hardware faces long-term continuous voltage stress, making electrical insulation a core design challenge. To prevent electrical breakdown over decades of operation, equalizers must meet the high-voltage isolation requirements of EN 50124, the standard for insulation coordination in railway systems up to 25 kV [46,47].

2.2. Stationary Energy Storage Applications

Stationary BESSs are core infrastructure for smoothing power fluctuations from wind and solar generation [48,49]. For stationary applications, the core design priority shifts from the power density requirement of vehicles to long-term economic performance, measured by the levelized cost of storage (LCOS) [50,51]. LCOS represents the total lifecycle cost per unit of delivered energy and is strongly affected by battery degradation, round-trip efficiency, and auxiliary energy consumption.

In stationary applications, the equalization strategy directly influences LCOS through three coupled mechanisms: equalization energy loss, thermal management burden, and the achievable service lifetime of the battery pack. Unlike electric vehicles, stationary storage systems typically operate over long service durations with continuous cycling, meaning that even small energy losses from the equalization circuit can accumulate into significant lifetime energy and cooling costs. Consequently, equalization design in stationary systems prioritizes long-term efficiency and aging management rather than compactness or peak power density.

From the perspective of operational characteristics, stationary BESSs can be broadly categorized into energy-oriented and power-oriented systems. In addition, both categories may employ second-life batteries, which introduce significantly increased cell heterogeneity and impose more stringent requirements on equalization and state estimation [52].

2.2.1. Energy-Oriented Stationary Storage

For energy-oriented installations such as large-scale BESS and microgrids for renewable integration, the main challenge comes from the huge system scale and large number of parallel cell branches. In these systems, LCOS is highly sensitive to round-trip efficiency and heat generation. As shown in Figure 4, stationary storage typically consists of large-scale battery packs connected in parallel [53]. Equalization systems in this field must not only reduce continuous heat dissipation from passive resistors, but also manage parallel current equalization to suppress circulating currents and uneven aging across different branches [54].

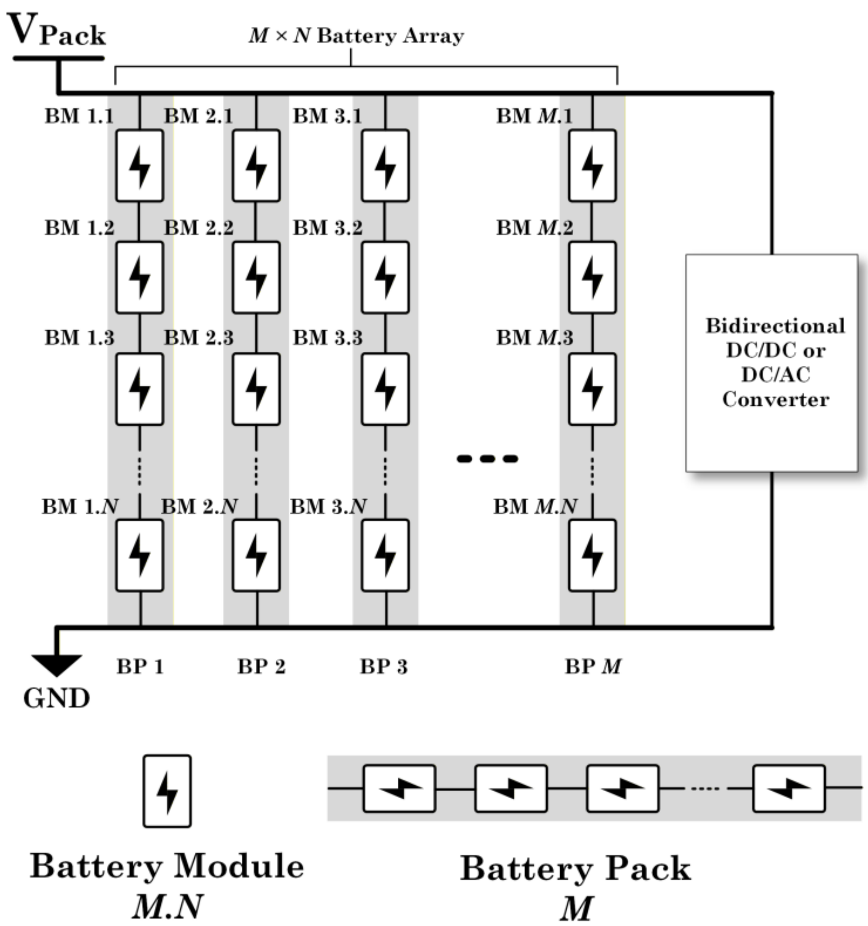

Figure 4. Battery energy storage system with multi-pack architecture.

2.2.2. Power-Oriented Stationary Storage

For power-oriented applications such as data center UPS and grid frequency regulation, systems operate under frequent high-rate charge–discharge cycles [55]. Rapid polarization and parameter inconsistency can cause individual cell voltages to approach safety limits under fast power dispatch conditions. Since passive equalization provides limited balancing current and cannot dynamically redistribute energy during operation, it is less effective in mitigating transient voltage divergence. Therefore, these fast-response scenarios require high-throughput active equalization architectures capable of real-time energy redistribution to ensure stable grid-level operation.

2.2.3. Second-Life Battery Storage

Repurposing retired EV batteries (which typically retain 70% to 80% of their initial capacity) for stationary storage is commercially attractive, but brings unique equalization challenges [56]. Compared with new batteries, second-life batteries have much larger parameter dispersion, imposing far stricter requirements on equalization performance.

Retired batteries have extreme inconsistency across multiple key parameters: first, non-linear aging leads to more than 20% capacity difference between individual cells in the same pack; second, uneven internal resistance growth causes localized hotspots and large voltage deviations under the same load; third, different self-discharge rates lead to rapid imbalance even during standby [57,58].

Traditional passive equalization is unsuitable for this scenario: the typical 100 mA passive equalization current is far too small to compensate for the 10-20 Ah capacity gaps common in second-life modules, and can easily misjudge cell status, leading to incorrect equalization and accelerated battery aging.

Therefore, equalization systems for second-life batteries must meet the following specialized design requirements:

(1) High equalization throughput: sufficient equalization current independent of small voltage differences, to complete charge redistribution within the short charge/discharge windows of stationary BESS;
(2) SOH-aware control logic: track the SOH and internal resistance of each cell in real time, to avoid pushing degraded weak cells beyond their safe operating limits [59];
(3) High fault tolerance: support real-time isolation or bypass of severely degraded cells, to ensure that a single failed cell does not disable the entire string, maintaining continuous system availability.

2.3. Aerospace and Satellite Missions

The operational environment of space missions imposes strict constraints on equalization systems, characterized by high-vacuum conditions, intense ionizing radiation, and zero maintainability. For instance, low earth orbit (LEO) satellites undergo frequent charge-discharge cycles, typically around 16 times per day [60]. This intense cycling requires the equalization system to maintain high precision and rapid response within very narrow orbital windows to prevent minor cell imbalances from escalating over time. Beyond cyclic stress, the radiative environment requires all semiconductor devices in the equalization circuit to be radiation-hardened to mitigate the effects of total ionizing dose (TID) and single event effects (SEE) [61].

Thermal management is another core challenge in the vacuum space environment. Without atmospheric convection, heat generated by equalization energy dissipation can only be removed through thermal conduction and radiation. This requires extremely high equalization efficiency to avoid localized hotspots, which would accelerate cell aging and threaten pack stability [62]. Finally, since space missions are completely unmaintainable, equalization systems must eliminate all single points of failure, requiring redundant energy paths and autonomous fault isolation capabilities.

2.4. Summary

To systematically map the operational boundaries of battery equalization systems, Table 1 benchmarks the divergent priorities across major application domains. It is evident that a "one-size-fits-all" design strategy is fundamentally unfeasible due to the shifting weighting of performance metrics across different sectors.

In the transportation domain, including passenger EVs, micro-mobility, UAVs and rail transit, the core priorities are high power density, fast dynamic response and long-term insulation reliability. Equalization circuits in this field must handle high-rate transients, cell polarization and electrical noise, while meeting strict space/weight constraints or high-voltage safety standards. In contrast, stationary energy storage and second-life battery applications are mainly driven by LCOS optimization and total energy throughput. For these large-scale systems, the design focus is on reducing energy losses from the equalization circuit, suppressing circulating currents in parallel branches, and managing the extreme parameter inconsistency of retired cells. Finally, specialized aerospace and satellite missions have the most stringent requirements: zero single-point failure, autonomous fault isolation, and vacuum-adapted thermal management, where long-term reliability and radiation immunity far outweigh initial hardware costs.

Ultimately, battery equalization system design is a multi-dimensional engineering trade-off among equalization speed, energy efficiency, hardware complexity, and lifetime reliability.

Table 1. Comprehensive comparison of application scenarios and design requirements for battery equalization systems.

Category	Application Scenario	Battery Chemistry	Scale & Configuration	Design Priorities	Key Challenges
Transportation	Passenger EVs (EV/HEV/PHEV) [27–35]	NMC [1], LFP [2]	350–800 V; 60–100 kWh; 96–200 S	Driving range extension, pack cycle life, high response speed, power density	High-rate dynamic transients, cell polarization, electrical noise, spatial and weight limits
	Micro-mobility (e-Bikes/Scooters) [36–38]	LFP, NMC	36–72V; 1–5 kWh; 10–20 S	High cost-performance ratio, low component count, high silicon integration	Cost sensitivity, manufacturing cost, compact form factors
	Unmanned Aerial Vehicles (UAVs) [39,41]	Li-Po [3], NMC	12–50 V; 0.05–5 kWh; 3–12 S	Specific power (power-to-weight ratio), low latency, rapid transient response	Extreme C-rate fluctuations, rapid voltage fluctuations, weight-sensitive endurance
	Rail Transit & Special Vehicles [42,45–47]	Fuel cells + Supercaps + Li-ion (HESS)	750–1500 V; Large-scale configurations	Long-term insulation integrity, high-voltage isolation (EN 50124), 20–30 year safety lifecycle (EN 50126)	Continuous high-voltage stress, electrical breakdown risks, energy and power synergy
Grid & Stationary	Energy-oriented BESS & Microgrids [48–52,54]	LFP, Sodium-ion	1000–1500 V; MWh to GWh level; Thousands of cells	LCOS optimization, round-trip efficiency, parallel current equalization	Long energy transfer paths, cumulative path losses, circulating currents, extra cooling load
	Power-oriented Services (UPS/Frequency Regulation) [55]	LFP, LTO [4], Lead-acid	48–400 V; 10 kWh–500 MWh; 16–110 S	High-throughput active equalization, grid operational stability	High-rate charge-discharge profiles, rapid cell polarization
	Second-life Batteries [56–59]	Retired LFP/NMC	48–1500 V; Flexible clusters	High current throughput independent of voltage gaps, SOH-aware coordination, real-time isolation or bypass	Extreme parameter heterogeneity, $> 20\%$ capacity difference, internal resistance hotspots, uneven self-discharge
Specialized	Aerospace & Satellite Missions [63,64]	NCA [5], NMC, LFP	28–100 V; 0.5–50 kWh; 8–28 S	High equalization precision, zero single-point-of-failure reliability, radiation hardness (TID/SEE), autonomous fault isolation	Vacuum thermal conduction and radiation, high-frequency orbital cyclic stress (16 cycles/day), zero maintainability

[1] NMC = Nickel Manganese Cobalt Oxide; [2] LFP = Lithium Iron Phosphate; [3] Li-Po=Lithium Polymer Battery; [4] LTO = Lithium Titanate Oxide; [5] NCA = Nickel Cobalt Aluminum Oxide.

3. Topological Evolution of Equalization Hardware

Table 2 summarizes all mainstream battery equalization hardware topologies, comparing their core energy transfer mechanisms, advantages, and inherent limitations for large-scale applications.

Table 2. Comparative analysis of hardware topologies for battery equalization.

Topology Category	Energy Transfer Medium	Primary Physical Advantages	Key Inherent Limitations
Passive Dissipative [65]	Resistors	Simple structure, high reliability, no magnetic components.	Inherent energy waste; heat generation creates severe thermal management burden.
Capacitor-Based (SC/RSC) [66–71]	Capacitors	High power density (no magnetic components).	Hard-paralleling inrush current; equalization speed decreases exponentially with shrinking voltage difference.
Inductor / Converter-Based [72–80]	Inductors	Fully controllable equalization current independent of voltage difference.	Trade-off between inductor volume and current ripple; distributed architectures have high control complexity.
Transformer-Based [81–87]	Shared Magnetic Core	Provides galvanic isolation; supports multi-port energy transfer.	Limited winding space inside the magnetic core prevents large-scale expansion; winding mismatch causes magnetic asymmetry in large packs.
Capacitively Coupled [88–91]	AC Coupling Capacitors	Low physical volume, excellent modular scalability, no bulky magnetics.	Requires precise phase synchronization of all AC link circuits.

3.1. Passive Dissipative Topologies

Passive equalization is the simplest and most mature equalization topology, which uses parallel resistor-switch networks to consume excess energy from high-SOC cells in the form of heat [65]. Although this method inherently wastes energy and increases thermal management burden, its simple structure, high reliability, and no requirement for magnetic components make it the mainstream choice for cost-sensitive scenarios such as micro-mobility and low-end consumer electronics. However, as battery packs continue to increase in capacity and power, the large amount of heat generated by equalization resistors has become an insurmountable physical bottleneck. This limitation directly drives the development and application of non-dissipative active equalization topologies in large-scale systems.

3.2. Capacitor-Based Topologies and Resonant Improvement

Switched-capacitor (SC) topologies transfer energy by periodically switching a bridging capacitor between different cells [66–71]. Although SC topologies eliminate bulky magnetic components and achieve high power density, basic SC designs have two critical inherent limitations [92].

(1) Hard-paralleling inrush current: the transient current is only limited by the tiny parasitic loop resistance R_{loop}, so connecting two cells with voltage difference will generate large current spikes with high di/dt and strong electromagnetic interference (EMI) radiation, bringing severe thermal and switching stress to MOSFETs and accelerating battery degradation [93].

(2) Voltage difference dependency: the equalization speed of basic SC circuits decreases as the cell voltage difference ΔV shrinks [94].

To solve both the inrush current problem and voltage dependency, resonant switched-capacitor (RSC) topologies were proposed. By adding a small resonant inductor, RSC circuits shape the transfer current into a near-sinusoidal waveform, achieving zero-current switching (ZCS). This greatly reduces switching losses and completely eliminates the hard-switching current spikes [95].

3.3. Inductor and Converter-Based Topologies

To achieve controllable equalization currents, inductor-based topologies, including Buck-Boost, Cuk, and SEPIC converters, operate as dedicated DC/DC converters regulated via pulse-width modulation (PWM) [72–74]. By utilizing inductors as the primary energy transfer medium, these configurations successfully eliminate the severe inrush currents inherent to switched-capacitor circuits. However, in practical high-density implementations, the hardware requires a tight trade-off between the physical volume of the equalizing inductors and the resulting current ripple amplitude. Furthermore, advanced converter-based equalization systems, such as dual active bridge (DAB) [75,76] and resonant converters [77–80], have been introduced to enable flexible multi-cell energy routing. These architectures use a centralized converter paired with a large selection switch matrix to connect arbitrary target cells to the converter ports. This design avoids the control complexity of distributed multi-converter architectures, but introduces new challenges in terms of high gate drive losses and meeting wide voltage conversion ratio requirements.

3.4. Transformer-Based Topologies

As shown in Figure 5a, transformer-based topologies use magnetic coupling to provide isolation and transfer energy among cells [81–87]. In multi-winding designs, cells are magnetically coupled through a shared core. Depending on the specific circuit, energy can be transferred directly from C2C, or distributed to the lowest-voltage cell.

However, the main limitation of this topology is physical scalability. For large battery packs, manufacturing a single transformer with many windings is technically challenging. The physical window area of the magnetic core strictly limits the number of secondary windings that can be added. Furthermore, it is practically impossible to manufacture numerous windings with perfectly identical structures. This structural inconsistency leads to poor magnetic symmetry, making it impossible to achieve effective equalization in large-scale applications.

3.5. Capacitively Coupled Topologies and Distributed Energy Routing

To overcome the scalability bottleneck of multi-winding transformers and the high switch count limitation of converter-based topologies, recent research has proposed capacitively coupled equalization architectures [88–90]. Figure 5b shows the structure of capacitively coupled topologies. These topologies are the dual of transformer-coupled equalization structures. Unlike traditional DC-coupled equalizers, these topologies use AC coupling capacitors as the core energy transfer medium, eliminating the need for bulky magnetic components and large selection switch matrices.

Replacing magnetic cores with lightweight coupling capacitors significantly reduces system volume and improves power density. This architecture also supports modular large-scale expansion. The structure allows all cells to exchange energy bidirectionally through a shared distributed AC link and completely bypasses the manufacturing and scalability limitations of multi-winding transformers.

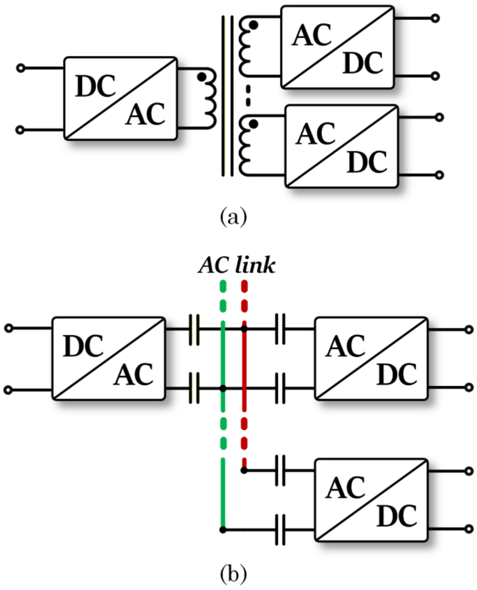

Figure 5. (**a**) Multi-winding transformer based multiport architecture. (**b**) Capacitively-coupled multiport architecture.

4. System-Level Architectures and Energy Routing

While hardware topologies determine the physical limits of energy conversion at the component level, the system architecture dictates the macroscopic energy routing paths across the entire battery pack. As illustrated in Figure 6, battery equalization structures can be systematically categorized into five main types [96]: adjacent cell-to-cell (C2C) [97,98], energy buffer-based cell-to-cell (EBC2C) [6,99], direct cell-to-cell (DC2C) [100–102], hierarchical module equalizer (HME) [103–106], and stack-to-cell (S2C) [107–114].

4.1. Cell-to-Cell (C2C) Architectures

The earliest equalization architectures are adjacent C2C configurations. As shown in Figure 6a, an independent DC/DC converter is connected between every two adjacent cells. This structure minimizes voltage stress and component ratings, but has a fundamental path-length bottleneck. Energy can only be transferred between immediate neighboring cells. As a result, energy transfer between distant cells requires cascaded transfer through multiple converters, leading to high cumulative losses and extremely long equalization time [115].

As illustrated in Figure 6b, an energy buffer-based C2C (EBC2C) equalizer employs a shared energy medium such as an inductor or LC network alongside a switching matrix, enabling direct energy transfer between any two cells regardless of physical distance. However, this architecture has a severe concurrency bottleneck. Since the shared buffer can only process one pair of cells at a time, the system must operate sequentially via time-division multiplexing, which fundamentally limits the overall equalization speed [116]. Alternatively, as illustrated in Figure 6c, the centralized energy buffer can be replaced by a dedicated DC/DC converter to achieve the same energy routing capability [117].

Further variations of C2C include DC-coupled (Figure 6d) and multiport AC-coupled (Figure 6e) architectures. The DC-coupled approach requires two full DC-AC-DC stages per transfer, resulting in four power conversion steps that degrade end-to-end efficiency [118]. Conversely, the multiport-AC-coupled structure processes differential power through a single intermediate AC stage, effectively reducing the conversion steps. Nevertheless, both variations share the same inherent limitation of DC2C systems: they typically lack concurrent multi-cell routing capabilities. Furthermore, allocating a dedicated half-bridge or full-bridge to every cell drastically multiplies the number of high-frequency active switches, significantly complicating the gate drive circuitry, increasing gate drive power consumption, and increasing system-level failure risks.

Further variations of C2C include DC-coupled (Figure 6d) and multiport AC-coupled (Figure 6e) architectures. The DC-coupled approach requires two full DC-AC-DC stages per energy transfer, resulting in four power conversion steps degrading end-to-end efficiency [118]. Conversely, the multiport AC-coupled structure processes differential power through a single intermediate AC stage, effectively reducing conversion steps. However, AC-coupled circuits require precise phase synchronization across all branches to ensure normal operation.

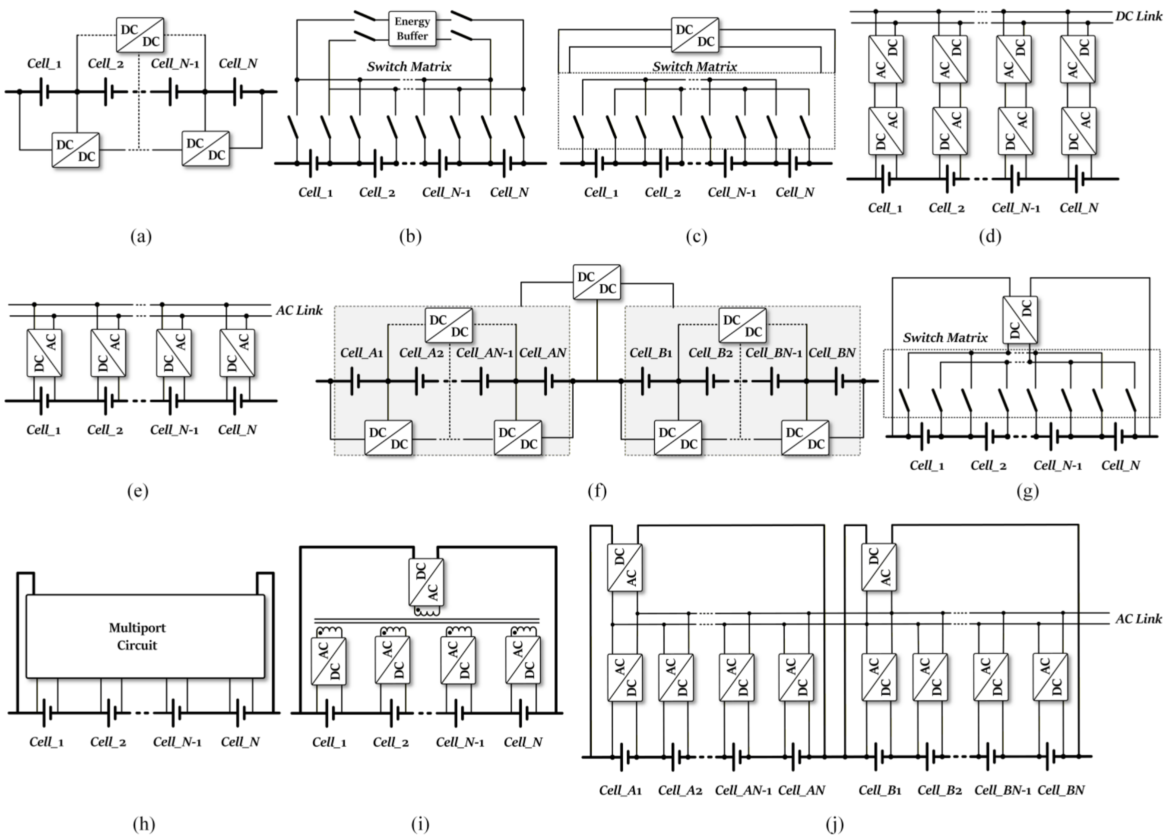

Figure 6. Block diagrams of a few equalization structures: (**a**)Adjacent cell-to-cell equalizer; (**b**) Energy buffer based cell-to-cell equalizer; (**c**) Converter based cell-to-cell equalizer; (**d**) DC-coupled cell-to-cell equalizer; (**e**) Multiport-AC-coupled cell-to-cell equalizer; (**f**) Hierarchical module equalizer; (**g**) DC-DC converter with selective switches (DCSS) based stack-to-cell equalizer; (**h**) Multiport circuit based stack-to-cell equalizer; (**i**) Multiwinding transformer coupling-based S2C equalizer; (**j**) Shared AC link stack-to-cell equalizer.

4.2. Hierarchical Module Equalization (HME)

To solve the path-length inefficiency problem of adjacent C2C architectures, large-scale battery systems usually adopt hierarchical module equalization (HME).

As shown in Figure 6f, HME uses multi-layers DC/DC converters to split the equalization task into intra-module equalization and inter-module equalization. This structure provides flexible energy routing paths. However, this architecture requires converters at different tiers to operate synchronously, so its core challenge is high control complexity [119].

4.3. Stack-to-Cell (S2C) Routing

Stack-to-Cell (S2C) architectures treat the entire battery pack as a bulk energy source to directly charge the lowest-voltage cells [120]. This macroscopic routing path inherently eliminates the cascading transfer delay problem of adjacent C2C architectures.

As illustrated in Figure 6g, a DC switching selection (DCSS) structure connects a shared DC/DC converter to individual cells via a switch matrix. While this implementation requires only one power converter, the required switch matrix scales poorly with pack size. Deploying a centralized multiplexer demands a large number of selector switches, which complicates the driving circuitry and increases the risk of single-point failures. More critically, the shared converter creates a structural concurrency bottleneck, allowing only one cell to be equalized at a time.

To eliminate the selector matrix and enable concurrent multi-cell equalization, isolated multiport circuits (Figure 6h) are utilized. A prevalent example (Figure 6i) is the multi-winding transformer, where the primary is connected to the stack and each secondary winding is dedicated to a specific cell [121]. However, as discussed in Section III, centralized multi-winding structures face severe physical scalability limits. It is practically impossible to manufacture a large number of identical windings on a single magnetic core, which limits the application of multiport S2C architectures in large-scale energy storage systems [122].

As shown in Figure 6j, the AC-link architecture is another S2C configuration. In this structure, cell-level AC-DC converters and module-level DC-AC converters are connected to a shared high-frequency AC link. This architecture allows energy transfer between any cells regardless of physical location, and supports simultaneous energy distribution among multiple modules and cells. For example, battery modules can feed power into the shared AC link, and multiple low-voltage cells across different modules can absorb this energy at the same time.

4.4. Comparative Evaluation and Operational Suitability

The selection of an equalization architecture depends on both hardware limitations and the spatial distribution of cell SOC mismatch within the pack. As the mismatch pattern changes, the efficiency and control complexity of different architectures also change.

4.4.1. Concentrated Mismatch (Single-Cell Depletion)

When a single cell has a significantly lower SOC than the rest of the pack, the centralized S2C architecture provides the most direct routing path. It utilizes the entire pack to transfer energy directly to the target cell in a single step. In contrast, an adjacent C2C architecture requires energy to pass through multiple intermediate cells, which increases cumulative conduction losses and control complexity.

4.4.2. Random and Dispersed Mismatch

In large-scale or second-life battery systems, SOC mismatch is often randomly distributed across the pack. Under these conditions, adjacent C2C architectures suffer from long transfer paths and slow equalization speeds. To address this, HME or Hierarchical AC-Link (Shared-Bus) architectures are more practical. Through a shared bus, they allow multiple healthy modules to simultaneously transfer energy to multiple weak cells, without having to process the energy transfers one by one.

Table 3 summarizes the physical trade-offs of these architectures. While advanced shared-bus architectures resolve the physical routing bottlenecks of C2C and S2C, managing their concurrent power flows introduces new control challenges. Solving these synchronization and circulating current issues requires transitioning from basic rule-based logic to system-level optimization algorithms.

Table 3. System-level comparative analysis of energy routing architectures.

Routing Architecture	Energy Routing Path	Concurrent Capability	System Scalability	Key Control & Hardware Challenges
Adjacent C2C [97,98]	Cascading transfers step-by-step between immediate physical neighbors.	Multipleadjacent pairs can operate simultaneously; each transfer remains local to neighboring cells.	Poor; path length increases linearly with pack size.	High cumulative conduction losses; extremely long equalization time for distant cells.
Buffer-Based & Direct C2C [6,99–102]	Direct transfer via shared energy medium or dedicated point-to-point converters.	Sequential operation only, limited by time-division multiplexing.	Poor; limited by exponential complexity of large switch matrices.	Very high switch count; complicates gate drive design and increases failure risk.
Hierarchical (HME) [103–106]	Split into independent intra-module and inter-module equalization loops.	Supports simultaneous operation across different independent tiers.	Excellent modularity; supports subsystem expansion without global redesign.	Requires precise synchronization of converters across multiple tiers.
Centralized S2C (DCSS Multiplex) [107,108]	Direct single-step transfer from the full pack to a single target cell.	Strictly sequential; only one cell can be equalized at a time.	Poor; centralized multiplexer layout does not scale to large packs.	High single-point failure risk; requires complex centralized switch matrix drive.
Multi-Winding Multiport S2C [109–112]	Bulk energy redistribution from stack to cells via isolated secondary windings.	High concurrency; supports simultaneous charging of multiple cells.	Strictly limited; limited winding space inside magnetic core prevents large-scale expansion.	Extremely high manufacturing difficulty; structurally unsuitable for large systems.
AC-Link S2C [113,114]	Position-independent cross-module routing via a universal high-frequency AC link.	Highly flexible; supports concurrent multi-to-multi energy transfer.	Excellent parallel scalability; no centralized magnetic or switch bottlenecks.	Requires high-frequency phase synchronization and circulating current suppression.

5. Performance Evaluation Metrics and Analytical Benchmarking

Many existing studies evaluate battery equalizers based on specific test conditions or absolute convergence times. However, convergence time depends heavily on battery capacity, making it difficult to objectively compare different architectures. To establish a standardized baseline, equalization systems should be evaluated using analytical models based on path efficiency and system-level throughput [123].

5.1. Path-Dependent System Efficiency (η_{sys})

Most literature defines equalization efficiency based on a single converter stage (η_{stage}). However, in a multi-cell architecture, the actual system-level efficiency (η_{sys}) is path-dependent.

Assuming an identical conversion efficiency η_{stage} for each power stage, the effective system efficiency between a source cell i and a target cell j decays exponentially with the number of conversion steps (k_{path}):

$$\eta_{sys}(i,j) = \prod_{m=1}^{k_{\text{path}}} \eta_{\text{stage},m} \approx \left(\eta_{\text{stage}}\right)^{k_{\text{path}}} \tag{1}$$

For adjacent C2C architectures (Figure 6a), energy must pass through $k_{path} = |i - j|$ converters, causing high energy loss for distant cells. For shared-AC-link architectures (Figure 6e), energy transfer requires two steps (cell-to-link, then link-to-cell), resulting in a constant efficiency of $\eta_{sys} = (\eta_{stage})^2$ regardless of physical distance. S2C architectures require only one step ($k_{path} = 1$).

5.2. Architecture-Level Concurrency Throughput

To objectively evaluate equalization speed independent of battery capacity, the evaluation must be based on the system-level equalization throughput (P_{sys_eq}). For active equalization circuits, this throughput is defined as the total power injected into the undercharged target cells:

$$P_{sys\_eq} = \sum_{i \in \mathbb{C}_{\text{target}}} V_i I_{eq,i}(V_i) \tag{2}$$

where $\mathbb{C}_{target}$ is the subset of undercharged cells that the hardware can charge at the same time. $I_{eq,i}(V_i)$ is the current injected into target cell i. Depending on the control characteristics, this may be a constant value or a function of the cell voltage V_i.

By applying this formula, the performance boundaries of different routing architectures can be analytically distinguished:

5.3. Topology-Level Concurrency Throughput

5.3.1. Actively Controlled Single-Target Architectures

For centralized architectures like DCSS (Figure 6g), the current is actively regulated to a constant reference value (I_{ref}), independent of the cell voltage:

$$I_{eq,i} = I_{\text{ref}} \quad (\text{independent of } V_i) \tag{3}$$

However, the switch matrix only allows one cell to be balanced at a time. Therefore, $\mathbb{C}_{target}$ contains only one cell, and the total system throughput is simply:

$$I_{sys\_eq,\,\text{single}} = I_{\text{ref}} \tag{4}$$

If M cells need equalization, they must be processed one by one. This sequential operation limits the global equalization speed during pack-level mismatches.

5.3.2. Localized Adjacent C2C Architectures

In adjacent C2C structures (Figure 6a), multiple cells can be balanced at once. However, to move energy across a physical distance of k cells, the same energy must pass through k intermediate converters. Accounting for this routing process, the effective global throughput decreases significantly:

$$I_{sys\_eq,\text{adjacent}} = \frac{1}{k} \sum_{i \in \mathbb{C}_{\text{target}}} I_{eq,\text{local}} \quad (5)$$

As the distance k increases, the effective throughput drops, making it inefficient for long battery strings.

5.3.3. Shared-Link (Distributed) Architectures

Shared-link architectures (Figure 6d,e) connect all cells to a common AC or DC link via dedicated converters. Because these converters can actively step up or step down the voltage, the equalization current is not merely driven by the raw voltage difference between the bus and the cell.

Instead, the converter applies a controllable conversion ratio M_i. The equivalent voltage interfacing the bus becomes a modulated function of the cell voltage ($M_i \cdot V_i$). Consequently, the current injected into the target cell is determined by the control variable rather than the physical voltage deviation:

$$I_{eq,i} = f(V_{\text{bus}},\ M_i \cdot V_i,\ Z_{eq}) \quad (6)$$

Furthermore, if these distributed converters operate under closed-loop current control, they can actively regulate the injection current to a nominal reference value (I_{nom}). The total system-level throughput becomes the sum of all actively regulated channels:

$$I_{sys\_eq,\text{distributed}} = \sum_{i \in \mathbb{C}_{\text{target}}} I_{\text{nom},i} \quad (7)$$

Since the shared link allows $\mathbb{C}_{target}$ to include all undercharged cells simultaneously, this concurrent multi-port operation yields a significantly higher total system throughput compared to single-target architectures.

5.4. Control, Sensing, and Communication Overhead (O_{ctrl})

The feasibility of an equalization system depends on its control complexity. The total control overhead (O_{ctrl}) can be modeled as a function of the active switch count (N_{sw}) and the algorithmic complexity (L_{ctrl}).

$$O_{\text{ctrl}} = f(N_{sw},\ L_{\text{ctrl}}) \quad (8)$$

The number of active switches determines the required number of independent PWM channels and gate drivers. In adjacent C2C architectures, N_{sw} scales linearly with the number of cells. The complexity of the control algorithm is mainly determined by the routing objective and the regulation requirements. Open-loop control uses fixed switching frequency and duty cycle, which has the lowest computational burden and does not require dynamic feedback or real-time state measurement. Conversely, closed-loop regulation requires continuous feedback to actively control the energy transfer. In such systems, managing multi-channel voltage and current sensing alongside compensator execution naturally increases the computational requirements.

6. Impact of OCV-SOC Characteristics on Equalization Difficulty

The difficulty of implementing effective cell equalization is highly correlated with the open-circuit voltage versus state-of-charge (OCV-SOC) characteristics of electrochemical energy storage devices. In voltage-based equalization architectures, the voltage discrepancy between cells serves as the primary driving force for equalization currents. Consequently, the slope of the OCV-SOC curve, denoted as $dV/dSOC$, inherently determines the sensing resolution required and the achievable equalization accuracy. Based on the quantitative analysis presented in Table 4, the equalization difficulty can be systematically classified into three distinct categories according to the voltage variation rate in the primary operating range (20–80% SOC): high < 5 mV/%), moderate (5–10 mV/%), and low > 10 mV/%.

6.1. High Equalization Difficulty: Flat Voltage Plateau Characteristics

Devices with extremely flat OCV-SOC curves in the primary operating range present the most significant challenge for equalization. As observed in Table 4, the lithium iron phosphate (LFP) battery, lead-acid battery, and lithium titanate (LTO) battery all fall into this category, with slopes of 1.67 mV/%, 2.0 mV/%, and 4.17 mV/%, respectively [123–125]. In these extended plateau regions, a substantial SOC mismatch yields a negligible terminal voltage difference. This minuscule ΔV is easily overshadowed by measurement noise, sensor inaccuracies, and dynamic polarization voltages (such as ohmic drops and diffusion overpotentials). As a result, conventional voltage-based equalization topologies become highly ineffective in the mid-SOC range for these chemistries, often leading to false equalization triggering or premature termination.

6.2. Moderate Equalization Difficulty: Intermediate Slopes

The second category primarily comprises nickel-cobalt-manganese (NCM)-based lithium-ion batteries, which typically feature moderate $dV/dSOC$ slopes bounded between 5 mV/% and 10 mV/% [126,127]. The consistent and moderate slope of NCM batteries ensures that a meaningful SOC imbalance translates into a reliable, measurable terminal voltage difference (ΔV). This adequate error signal mitigates the impact of measurement noise and facilitates a stable convergence of equalization currents. Consequently, conventional voltage-based equalization topologies can operate effectively for NCM strings without strictly relying on computationally expensive, model-based SOC estimation algorithms.

Table 4. Comparison of OCV-SOC voltage variation and slopes for different electrochemical energy storage devices.

Energy Storage Device	Rated Voltage (V)	Operating Range (V)	0–20% Range (V)	0–20% Slope (mV/%SOC)	20–80% Range (V)	20–80% Slope (mV/%SOC)	80–100% Range (V)	80–100% Slope (mV/%SOC)
High Equalization Difficulty (<5 mV/%SOC)								
LFP Li-ion Battery [124]	3.2	2.5–3.65	2.5–3.2	35.0	3.2–3.3	1.67	3.3–3.65	17.5
Lead-Acid Battery [125]	2.0	1.92–2.18	1.92–2.0	4.0	2.0–2.12	2.0	2.12–2.18	3.0
LTO Li-ion Battery [126]	2.4	1.8–2.8	1.8–2.15	17.5	2.15–2.4	4.17	2.4–2.8	20.0
Moderate Equalization Difficulty (5–10 mV/%SOC)								
NCM523 Li-ion Battery [127]	3.7	3.0–4.2	3.0–3.6	30.0	3.6–3.95	5.83	3.95–4.2	12.5
NCM811 Li-ion Battery [128]	3.7	3.0–4.2	3.0–3.5	25.0	3.5–4.0	8.33	4.0–4.2	10.0
Low Equalization Difficulty (>10 mV/%SOC)								
Li-ion Capacitor (LIC) [129]	3.8	2.2–3.8	2.2–2.55	17.5	2.55–3.5	15.8	3.5–3.8	15.0
EDLC Supercapacitor [130,131]	2.7	0–2.85	0–0.6	30.0	0.6–2.1	25.0	2.1–2.85	37.5

6.3. Low Equalization Difficulty: Linear Capacitive Characteristics

Energy storage devices based on capacitive energy storage mechanisms, including lithium-ion capacitors (LICs) and electric double-layer capacitors (EDLCs), offer the lowest equalization difficulty, as their mid-SOC slopes consistently exceed the 10 mV/% threshold. LICs exhibit good linearity with a mid-range slope of 15.8 mV/%, while EDLCs reach 25.0 mV/% [128–130]. Due to their strict linear or semi-linear relationship between voltage and stored charge, any capacity or SOC imbalance directly produces a large equalization voltage difference. This strong ΔV enables even the simplest equalization circuits to achieve fast cell equalization, with minimal impact from current ripples or measurement noise.

6.4. Improved Equalization Performance in the Deep Discharge Region

A consistent trend is observed across all electrochemical energy storage devices in Table 4: the OCV-SOC slope ($dV/dSOC$) increases significantly in the deep discharge region ($0-20\%$ SOC). For example, the slope of LFP batteries rises from 1.67 mV/% in the mid-SOC range to 35.0 mV/% in the low-SOC region. As a result, voltage-based equalization circuits achieve much higher sensitivity and equalization performance in this range. This larger terminal voltage difference creates a strong driving force to quickly equalize under-charged cells. This inherent characteristic is especially beneficial for active equalization systems in large-scale energy storage, as it naturally prioritizes equalization of deeply discharged cells, acting as a key protective measure against irreversible over-discharge.

7. Future Outlook and Research Directions

Based on the systematic analysis in this review, future battery equalization systems will develop towards multi-function integration, high power density, modular scalability and chemistry-adaptive design. Six core research directions are identified as follows:

7.1. Equalization and Battery Diagnosis Hardware Fusion

Future equalization systems will realize deep integration with real-time battery diagnosis functions through hardware reuse. The equalization circuit can be used as an embedded excitation source, and the voltage and current data generated during the equalization process can be used to online diagnose battery SOH, internal resistance and aging state. This architecture eliminates the need for independent diagnosis hardware, significantly reducing the total system cost and hardware complexity.

7.2. High-Frequency Equalization Circuit Design

To reduce the volume and weight of passive components, future equalization circuits will develop towards high-frequency operation. By increasing the switching frequency to the MHz level, the size of magnetic components (inductors and transformers) and capacitors can be significantly reduced, greatly improving the power density of the equalization system. This is particularly important for space-constrained applications such as electric vehicles and aerospace systems.

7.3. Modular Scalable Equalization Architectures

Future equalization systems will adopt fully modular design to adapt to battery systems of different voltage levels. Modular architectures can be flexibly expanded according to system scale without global hardware redesign. At the same time, modular design can significantly reduce the voltage stress of power semiconductor devices, improving system reliability and reducing device cost.

7.4. High-Speed Equalization for High-Rate Discharge Scenarios

For high-rate discharge application scenarios such as electric vehicles and peak shaving energy storage, equalization speed will become a core performance indicator. Future research will focus on improving system-level concurrent equalization throughput, to achieve fast equalization during short charge-discharge intervals, ensuring that the system can maintain cell uniformity even under continuous high-rate operation.

7.5. High-Reliability Low-Switch-Count Topologies

To reduce system failure risk, future equalization topologies will minimize the number of active power switches. Reducing the number of switches not only reduces gate drive complexity and system cost, but also directly reduces the probability of single-point failures, significantly improving the long-term operational reliability of large-scale battery systems.

7.6. High-Precision Equalization for Flat OCV Curve Chemistries

As demonstrated in this review, LFP, LTO and lead-acid batteries with extremely flat OCV-SOC curves face fundamental equalization accuracy challenges. Future research will focus on high-precision voltage sampling and SOC-based equalization control strategies, to achieve accurate equalization for low-slope cell chemistries, which is the most urgent practical demand for large-scale LFP energy storage systems.

8. Conclusions

This paper presents a systematic review of battery equalization systems, addressing the limitations of existing reviews that focus predominantly on circuit-level topology optimization while neglecting architectural-level performance evaluation and standardized benchmarking.

First, this work quantifies the different equalization requirements for electric vehicles, grid energy storage, second-life batteries and aerospace applications, and clarifies that there is no universal optimal equalization solution. Architecture selection must be matched to application-specific performance requirements on cost, scalability and reliability.

Second, this review summarizes the technological evolution of equalization systems: from passive dissipation and adjacent cell-to-cell topologies to distributed energy routing architectures. This work shows that circuit-level efficiency improvements have limited effect in large-scale systems. Routing path and concurrent throughput are the core factors determining system-level equalization performance.

Furthermore, this work proposes a capacity-independent unified performance evaluation framework, based on system equalization throughput and control overhead. This framework eliminates performance comparison ambiguity caused by inconsistent test conditions and exaggerated current measurements in existing literature. This paper also quantifies the correlation between OCV-SOC characteristics and equalization difficulty, and establishes a clear matching rule between cell chemistry and suitable equalization architectures, which provides a theoretical basis for engineering scheme selection.

The future research directions outlined above will lay a foundation for the development of next-generation high-performance, highly scalable battery management systems.

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Author Contributions

Z.W.: conceptualization, methodology, investigation, visualization, and writing—original draft preparation; H.S.-H.C.: supervision, validation, project administration, funding acquisition, and writing—review and editing. Both authors have read and agreed to the published version of the manuscript.

Funding

This work was supported by the Green Tech Fund under Project GTF20202016 and Research Grants Council under project RIF R1004-24 from the Hong Kong Special Adminstraive Region, China.

Institutional Review Board Statement

Not applicable.

Informed Consent Statement

Not applicable.

Data Availability Statement

No new data were created or analyzed in this study. Data sharing is not applicable to this article.

Conflicts of Interest

The authors declare no conflict of interest.

Use of AI and AI-Assisted Technologies

During the preparation of this work, the authors used ChatGPT for language editing. After using this tool, the authors reviewed and edited the content as needed and take full responsibility for the content of the published article.

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