

Article

Energy-Aware Design and Performance Analysis of Through-Oxide Thermal Vias (TOTVs) via Finite Element Analysis and Driven Optimization

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Abstract: This study employs three-dimensional finite element analysis (FEA) to investigate the coupled thermo-mechanical behavior and electrical energy characteristics of Through-Oxide Thermal Via (TOTV) structures under thermal cycling conditions, with an emphasis on quantifying trade-offs between mechanical reliability and electrical efficiency. A unified three-dimensional thermo-mechanical and electrical modeling framework is established to capture stress concentration, deformation behavior, and geometry-dependent parasitic effects in a physically consistent manner, with observed trends showing qualitative agreement with prior TOTV-related studies. Single-objective optimization results indicate that geometric refinement can reduce the maximum principal stress from 119.54 MPa to 97.64 MPa, corresponding to an 18.3% relative improvement within the adopted modeling assumptions. However, such mechanically optimized configurations are accompanied by increased parasitic capacitance, leading to higher dynamic energy consumption. This observation quantitatively highlights the inherent conflict between structural integrity and electrical energy efficiency in dense TOTV arrays. To systematically explore this trade-off, a Multi-Objective Genetic Algorithm (MOGA) is employed to construct a Pareto-optimal design set. A representative compromise solution—characterized by a via radius of 21.246 μm , pitch of 69.172 μm , and copper thickness of 1.011 μm —achieves a 14.8% reduction in maximum principal stress and a 72% reduction in axial deformation (0.0156 μm), while avoiding the severe energy penalties observed in reliability-only optimizations. Rather than emphasizing absolute performance prediction, the proposed framework serves as an energy-aware design-space exploration methodology, providing quantitative insight into the relative severity of mechanical–electrical trade-offs for future high-density 3D integrated circuits and silicon photonics applications.

Keywords: energy loss reduction; through-oxide thermal via (TOTV); multi-objective optimization; finite element analysis (FEA); 3D integrated circuits

1. Introduction

Through-silicon vias (TSVs) have become a key enabling technology for three-dimensional integrated circuits (3D ICs), as they significantly shorten interconnect lengths, enhance integration density, and improve bandwidth and overall system performance [1–4]. By enabling vertical signal transmission through the silicon substrate, TSV-based architectures effectively overcome the limitations of conventional two-dimensional interconnects and provide a scalable solution for heterogeneous integration and high-performance computing systems.

Despite these advantages, the introduction of TSVs also brings substantial challenges associated with thermal management, mechanical reliability, and electrical parasitic effects. Copper-filled TSVs are widely adopted owing to their low electrical resistivity and high thermal conductivity; however, the pronounced mismatch in coefficients



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of thermal expansion (CTE) among copper, silicon, and surrounding dielectric materials induces significant thermo-mechanical stress and strain during fabrication and operation [5,6]. Excessive equivalent stress and strain may lead to interfacial delamination, dielectric cracking, and long-term reliability degradation, particularly under repeated thermal cycling conditions [7–9]. Consequently, mitigating thermo-mechanical reliability issues has become a critical concern in TSV structural design.

To address temperature rise and stress concentration in TSV-based systems, various thermal management strategies have been proposed, including optimized heat dissipation paths, thermal vias, and improved boundary condition design [7,10]. Thermal via concepts originally developed for high-power electronic packaging and photonic systems have demonstrated their effectiveness in reducing local hot spots and suppressing thermally induced mechanical failure [7,8]. In particular, through-oxide thermal vias (TOTVs) have attracted increasing attention as dedicated heat-conduction structures that can enhance vertical heat transport without interfering with electrical signal routing. Prior studies have shown that properly designed thermal via structures can significantly improve temperature uniformity and reduce thermally induced stress under realistic operating conditions [8,10].

However, most existing investigations on TSV, TGV, and thermal via structures rely primarily on simplified two-dimensional (2D) cross-sectional models [5,7,8]. While such models provide valuable physical insight and computational efficiency, they are insufficient to fully capture three-dimensional stress distributions, geometric interactions, and parasitic coupling effects in dense vertical interconnect configurations. This reliance on 2D approximations represents a significant theoretical gap, as it fails to account for the complex spatial interactions and non-uniform stress gradients present in real-world 3D architectures. Therefore, a transition toward high-fidelity three-dimensional (3D) modeling is not merely a numerical refinement but a theoretical necessity to accurately evaluate the thermo-mechanical reliability and electrical behavior of advanced interconnect systems.

Beyond thermo-mechanical reliability, the electrical characteristics of TSVs play a crucial role in determining system-level performance and energy efficiency. TSV geometry, including diameter, pitch, and dielectric configuration, directly affects equivalent resistance and parasitic capacitance, thereby influencing signal integrity, crosstalk, and timing behavior [11–14]. Analytical and semi-empirical models have been widely employed to estimate TSV parasitic parameters efficiently without resorting to full-wave electromagnetic simulations [12,13]. These studies consistently indicate that aggressive TSV scaling and increased TSV density can significantly exacerbate capacitive coupling and power noise [14,15]. To facilitate analytical estimation of mutual capacitance in dense TSV arrays, an effective coupling factor is commonly introduced, with reported engineering values typically ranging from 0.5 to 0.8 depending on geometry and dielectric configuration [16,17].

From an energy perspective, parasitic resistance and capacitance associated with TSVs contribute directly to switching energy dissipation and have become a non-negligible component of total power consumption in highly integrated 3D IC systems [18,19]. Recent works have highlighted that energy-aware interconnect design is essential for sustaining performance scaling in 3D ICs, particularly under high switching activity and dense vertical interconnect layouts [15,18,19]. In addition, power-aware and energy-efficient design methodologies have been increasingly emphasized in the broader context of sustainable electronic systems and green energy research [19–21].

Despite these advances, most existing studies still treat thermo-mechanical reliability and electrical energy performance as largely independent design objectives. Moreover, although three-dimensional modeling has been adopted in several recent TSV and TOTV investigations, such efforts are predominantly confined to mechanical reliability assessment or parametric trend analysis, without systematically incorporating electrical energy considerations into the design process. Consequently, the coupled influence of TSV and TOTV geometric parameters on stress, strain, and energy consumption has not yet been thoroughly examined within a unified three-dimensional framework.

The primary contribution of this work does not lie in proposing a new via structure, but rather in establishing an integrated modeling and optimization methodology that explicitly bridges mechanical reliability and electrical energy efficiency at the via-array level. In contrast to prior studies that investigate thermal–mechanical behavior or electrical parasitics in isolation, the present study incorporates electrical energy consumption as a co-equal design objective and couples it with mechanical performance metrics within a consistent three-dimensional physical framework.

Motivated by the limitations of these fragmented approaches, a comprehensive three-dimensional through-oxide thermal via (TOTV) modeling and optimization framework is proposed. Established thermal management concepts are extended from simplified two-dimensional representations to full three-dimensional geometries, enabling the simultaneous evaluation of spatial stress distributions, deformation characteristics, and parasitic electrical interactions under consistent geometric and boundary conditions. Furthermore, a systematic design-space exploration strategy is employed by integrating design of experiments (DOE), surrogate modeling, and a

multi-objective genetic algorithm (MOGA), allowing global trade-off relationships to be identified rather than relying on localized or single-objective optimization.

Rather than emphasizing absolute numerical improvements, this study focuses on elucidating the intrinsic trade-offs between structural integrity and electrical energy efficiency in dense TOTV arrays. The proposed framework is therefore positioned as a physically consistent design-space exploration and decision-support tool, providing quantitative guidance for balancing competing mechanical and electrical objectives in future high-density three-dimensional integrated circuits and silicon photonics applications.

2. Theoretical Modeling and Methodology

2.1. Geometrical Model and Design Variables

The structure under investigation is a three-dimensional Through-Oxide Thermal Via (TOTV) embedded within a silicon dioxide (SiO_2) matrix, as illustrated in Figure 1 [8]. The TOTV is composed of copper, with its bottom surface directly connected to the silicon substrate and its top surface attached to a copper heat spreader. In this configuration, the TOTV serves as a multifunctional vertical interconnect, providing an effective heat dissipation path while simultaneously influencing electrical energy performance through geometry-dependent parasitic effects.

The total length of the TOTV is fixed at $L = 9.22 \mu\text{m}$, corresponding to the representative vertical interconnect height in advanced 3D integrated circuit stacks. In order to decouple vertical scaling effects from lateral geometric interactions and to enable systematic interpretation of the coupled thermo-mechanical and electrical behaviors, the via length is held constant throughout this study.

Three primary geometric parameters are selected as design variables for optimization, including the TOTV diameter (D) ranging from 0.3 to $0.5 \mu\text{m}$, the TOTV pitch (p) ranging from 0.75 to $10 \mu\text{m}$ (corresponding to an array of 4 to 48 TOTVs distributed within a total lateral span of $37.703 \mu\text{m}$), and the heat spreader thickness (T) ranging from 0.1 to $1.0 \mu\text{m}$. The spacing between adjacent vias is defined as $g_p = 37.703/p - D$, which is employed in the mutual capacitance formulation to capture electrical coupling effects between neighboring TOTVs. The gap is not treated as an independent design variable, as it is fully determined by the selected diameter and pitch. This geometric configuration enables consistent three-dimensional evaluation of thermal, mechanical, and electrical behaviors within a unified structural framework.

Unlike conventional two-dimensional cross-sectional models, the present study adopts a full three-dimensional geometric representation. This enables accurate evaluation of spatial stress and strain distributions, deformation characteristics, and electrical parasitic interactions within dense TOTV arrays under consistent geometric and boundary conditions.

Although idealized periodic via arrays are considered, the proposed modeling and optimization framework is general and can be readily extended to alternative via lengths, non-uniform layouts, or heterogeneous stacking configurations by modifying the geometric parameters accordingly. The material properties employed in the simulations are summarized in Table 1 [8].

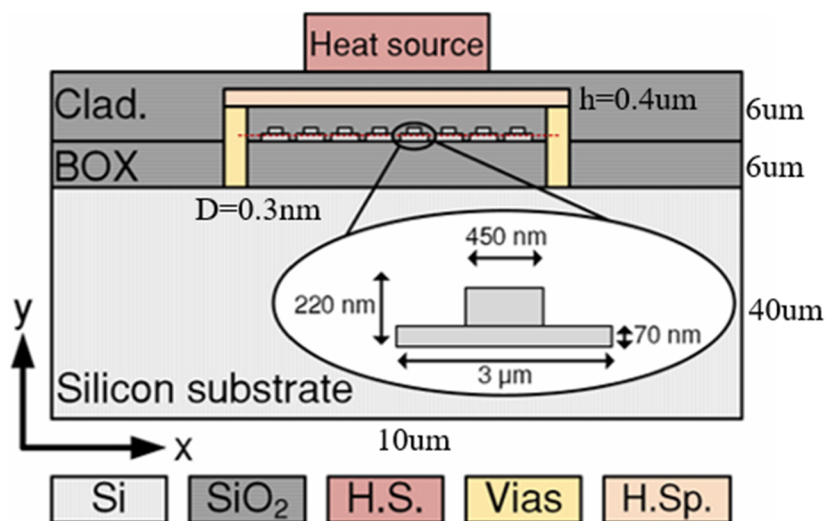


Figure 1. Schematic diagram of the 3D through-oxide thermal via (TOTV) structure with integrated heat spreaders and localized heat sources.

Table 1. Physical and thermo-mechanical material properties used in the FEA simulations.

Material	Thermal Conductivity (W/m·K)	Heat Capacity (J/K)	Density (kg/m ³)
Cu	400	385	8960
Si	148	700	2329
SiO ₂	1.4	730	2200

2.2. Boundary Conditions

For the thermo-mechanical analysis, the bottom surface of the silicon substrate is fixed in all translational directions to eliminate rigid body motion, while all remaining surfaces are allowed to deform freely. This constraint configuration ensures numerical stability while allowing the intrinsic thermo-mechanical responses of the TSV–TOTV structure to develop without artificial over-constraining.

The thermal boundary conditions are defined to represent a simplified yet physically consistent operating environment commonly adopted in early-stage design-space exploration studies. Specifically, the bottom surface of the silicon substrate is maintained at a constant reference temperature of $T_0 = 25\text{ }^{\circ}\text{C}$, serving as a thermal sink that approximates heat dissipation through the bulk substrate and underlying package layers. This boundary condition is imposed as a Dirichlet constraint to provide a stable thermal reference for comparative analysis.

All exposed external surfaces are subjected to natural convective heat transfer, with an ambient temperature of $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$ and a convection coefficient of $h_{\text{conv}} = 10\text{ W/m}^2\cdot\text{K}$. This value corresponds to free convection under still-air conditions and is widely used in numerical studies to represent passive cooling scenarios in the absence of forced airflow or liquid cooling mechanisms.

It is acknowledged that real 3D integrated circuit packages may experience spatially non-uniform temperatures, complex heat transfer paths, and varying convection coefficients depending on packaging configuration and operating conditions. However, the present boundary conditions are intentionally simplified to ensure consistency across all design cases and to enable meaningful comparison of relative trends in stress, strain, and energy-related metrics. While the absolute magnitudes of the thermal and mechanical responses may vary under more complex boundary conditions, the relative trade-off behaviors identified in this study are expected to remain qualitatively valid.

2.3. Electrical Modeling and Energy Consumption

To enable efficient design-space exploration without the prohibitive computational cost of full-wave electromagnetic simulations, compact analytical models are adopted to characterize the electrical behavior of the TOTV array. Rather than targeting absolute extraction of parasitic parameters, the electrical modeling in this study is intended to capture dominant physical trends and relative variations associated with geometric design changes, which is sufficient for comparative optimization purposes.

The electrical objective is formulated based on one resistance component and three capacitance components, following widely used analytical approximations for TSV-based interconnects.

2.3.1. Equivalent Electrical Resistance

The electrical resistance (R_{single}) of a single TOTV is expressed as [16,17,22]

$$R_{\text{single}} = L/(\rho * A) \quad (1)$$

where L is the via length, ρ is the electrical resistivity of copper, and A is the cross-sectional area of the via. This formulation follows classical conductor resistance theory and has been widely adopted in TSV resistance modeling. For p TOTVs connected in parallel, the equivalent resistance (R_{eq}) is:

$$R_{\text{eq}} = R_{\text{single}}/p \quad (2)$$

This parallel resistance assumption is appropriate for densely packed vertical interconnect arrays and is commonly used in energy-aware TSV analyses.

2.3.2. Capacitance Components and Energy Consumption

The total effective capacitance (C_{tot}) of the TOTV array is composed of three parasitic capacitance components, namely the mutual capacitance between adjacent vias, the TOTV-to-plane capacitance between the via and the heat spreader, and the self-capacitance between the via and the silicon substrate. These capacitance

components are modeled using compact analytical expressions to enable efficient parametric evaluation during optimization.

The mutual capacitance (C_m) represents the capacitive coupling between neighboring TOTVs through the surrounding silicon dioxide dielectric. Following established analytical TSV coupling models, the mutual capacitance is approximated as [16,17,22]:

$$C_m = k \cdot \epsilon_{ox} \cdot L \cdot D / g_p \quad (3)$$

where ϵ_{ox} is the permittivity of silicon dioxide, D is the via diameter, and g_p denotes the spacing between adjacent vias. The coefficient k is an empirical coupling factor introduced to account for non-uniform electric field distributions in dense via arrays. Reported engineering values of k typically range from 0.5 to 0.8 depending on geometry and dielectric configuration. In this study, $k = 0.6$ is adopted as a representative value.

This simplified form preserves the correct physical dependence on via diameter, length, and spacing, while avoiding logarithmic or hyperbolic functions that are incompatible with parametric optimization tools such as ANSYS DesignXplorer.

The coupling between the TOTV and the copper heat spreader is modeled as a TOTV-to-plane capacitance (C_{tp}), which is approximated using the parallel-plate capacitor formulation [22]:

$$C_{tp} = \epsilon_{ox} \cdot \pi \cdot (D/2)^2 / T \quad (4)$$

where T is the thickness of the heat spreader. This approximation is commonly employed when one conductor surface is significantly larger than the via cross-section and serves as an effective reference plane.

In addition, the self-capacitance (C_{self}) accounts for the electrical coupling between the TOTV and the conductive silicon substrate. It is expressed as [17]:

$$C_{self} = \epsilon_{Si} \cdot A / t_e \quad (5)$$

where $A = \pi \cdot (D/2)^2$, ϵ_{Si} is the permittivity of silicon and t_e denotes an effective coupling length. It should be emphasized that t_e does not correspond to a physical dielectric thickness but is introduced as an effective parameter to represent strong electrical coupling between the via and the conductive silicon substrate. Similar effective-distance concepts have been used in prior TSV modeling to capture substrate coupling effects without detailed semiconductor physics.

Based on the above definitions, the total effective capacitance is obtained as:

$$C_{tot} = C_{self} + C_m + C_{tp} \quad (6)$$

Consequently, the electrical energy consumption (E) per switching event is calculated as [16,18]:

$$E = C_{tot} \cdot V_{dd}^2 \quad (7)$$

This formulation represents the worst-case dynamic energy associated with charging and discharging the total effective capacitance and is widely adopted in interconnect-level energy comparison studies. Since all design cases are evaluated under identical voltage conditions, this definition enables a consistent and fair relative comparison of energy efficiency across different geometric configurations.

It should be noted that the electrical energy metric adopted in this work is intended as a relative performance indicator, rather than an absolute estimation of power consumption. Owing to the use of simplified analytical models for parasitic capacitance, the calculated energy values are not claimed to represent exact operating energy. Instead, they serve to systematically evaluate comparative trends and trade-off relationships between electrical efficiency and mechanical reliability within a unified modeling framework. This formulation is therefore appropriate for design-space exploration and multi-objective optimization purposes.

2.4. Multi-Objective Optimization

The optimization framework simultaneously evaluates mechanical reliability and electrical performance using normalized objective metrics. The mechanical objective function F_M is defined as the weighted combination of normalized maximum equivalent stress and normalized maximum equivalent strain, expressed as:

$$F_M = 0.5 \cdot (\text{normalized stress}) + 0.5 \cdot (\text{normalized strain}) \quad (8)$$

Similarly, the electrical objective function F_E is defined as the weighted combination of normalized equivalent resistance and normalized mutual capacitance:

$$F_E = 0.5 \cdot (\text{normalized } R_{eq}) + 0.5 \cdot (\text{normalized } C_m) \quad (9)$$

Based on these definitions, the overall objective function F_{total} is formulated as a weighted sum of the mechanical and electrical objectives:

$$F_{\text{total}} = w \cdot F_M + (1 - w) \cdot F_E \quad (10)$$

where w is the weighting factor representing the relative importance assigned to mechanical reliability. By varying w , different design preferences ranging from reliability-oriented to energy-oriented optimization can be systematically explored.

To efficiently explore the design space and construct surrogate models, Central Composite Design (CCD) was adopted to generate representative sampling points across the defined geometric parameter ranges. Based on these sampled design points, Response Surface Approximation (RSA) models were constructed to establish surrogate relationships between design variables and performance responses. These surrogate models significantly reduce the computational cost of repeated finite element simulations during optimization while maintaining sufficient predictive accuracy for trend evaluation.

Subsequently, a multi-objective genetic algorithm (MOGA), implemented in ANSYS DesignXplorer and based on the NSGA-II evolutionary framework, was employed to identify Pareto-optimal solutions and perform global trade-off analyses. The convergence of the optimization process was automatically monitored using built-in Pareto stability and convergence stability percentage criteria. Although a maximum of 20 iterations was permitted, convergence was achieved after 6 iterations, indicating stabilization of the Pareto front. In total, 5903 function evaluations were performed to obtain the final converged Pareto solution set. This systematic optimization procedure enables identification of global trade-off relationships between mechanical reliability and electrical energy efficiency, rather than relying on localized or single-objective optimization results.

3. Simulation Analysis and Validation

The numerical simulations were conducted using three-dimensional finite element analysis (FEA) within the ANSYS environment. The analysis workflow follows a systematic procedure encompassing geometry construction, material assignment, mesh generation, boundary condition definition, parametric setup, and numerical solution. Prior to the parametric and optimization studies, a mesh convergence analysis was performed to ensure numerical stability and minimize discretization-induced numerical errors. In addition, the spatial distributions of stress and strain were examined to identify critical regions and dominant mechanical responses under thermal loading.

The validation strategy in this study focuses on ensuring numerical stability and physical consistency of the proposed three-dimensional modeling framework. Mesh convergence analysis is employed to eliminate mesh-dependent numerical artifacts, while qualitative comparisons with commonly reported thermo-mechanical behaviors in TSV-related studies are used to verify the physical plausibility of the simulated stress concentration and deformation patterns. It should be emphasized that the present validation aims to support comparative trend analysis across different design configurations rather than absolute quantitative prediction of stress, strain, or energy values.

3.1. Mesh Convergence and Quality Verification

To strike a balance between numerical accuracy and computational efficiency, a mesh convergence study was conducted for the three-dimensional TOTV model. The maximum equivalent von Mises stress and maximum equivalent elastic strain were selected as the primary convergence indicators, as they directly reflect the critical thermo-mechanical responses governing structural reliability.

Table 2 summarizes the variations of the maximum equivalent stress and strain under progressively refined mesh sizes ranging from 4.0 μm to 2.0 μm , while Figure 2 illustrates the corresponding convergence trend of the maximum von Mises stress. At relatively coarse mesh sizes ($\geq 3.0 \mu\text{m}$), noticeable fluctuations in both stress and strain are observed, indicating insufficient spatial resolution. As the mesh is further refined, these responses gradually stabilize.

When the average element size is reduced from 2.5 μm to 2.0 μm , the variation in maximum von Mises stress is less than 0.1%, and the corresponding variation in maximum equivalent elastic strain is below 1%. This quantitative criterion confirms that numerical convergence has been achieved. Based on this observation, an average element size of 2.0 μm was selected for all subsequent simulations.

Using the selected mesh resolution, the final discretized model consists of 875,100 nodes and 617,387 second-order tetrahedral (Tet10) elements. The mesh quality characteristics are further evaluated in Figure 3. The

element quality distribution is predominantly concentrated in the high-quality range, with an average element quality of 0.81, indicating well-shaped elements and favorable numerical stability.

In addition, the average aspect ratio is 2.237, suggesting only moderate element stretching without severe distortion, while the average Jacobian ratio is 0.99, which is very close to the ideal value of unity. These mesh quality metrics confirm that the adopted mesh configuration provides a robust and reliable numerical foundation for the subsequent thermo-mechanical analyses and optimization studies.

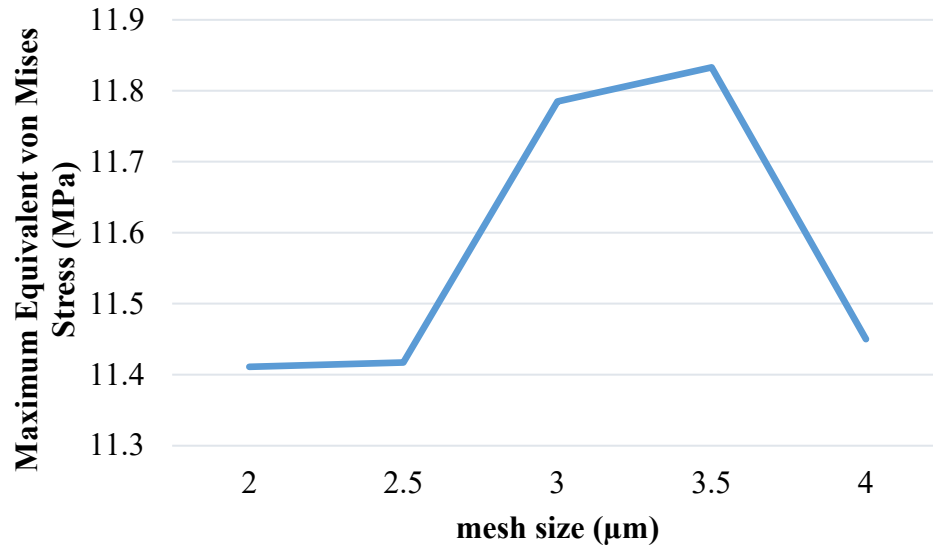


Figure 2. Mesh Convergence Analysis.

Table 2. The maximum equivalent von Mises stress and maximum equivalent elastic strain under different mesh sizes.

Mesh Size (μm)	2	2.5	3	3.5	4
Maximum Equivalent von Mises Stress (MPa)	11.411	11.417	11.785	11.833	11.45
Maximum Equivalent Elastic Strain	0.0001631	0.00016407	0.00016807	0.00016952	0.0001645

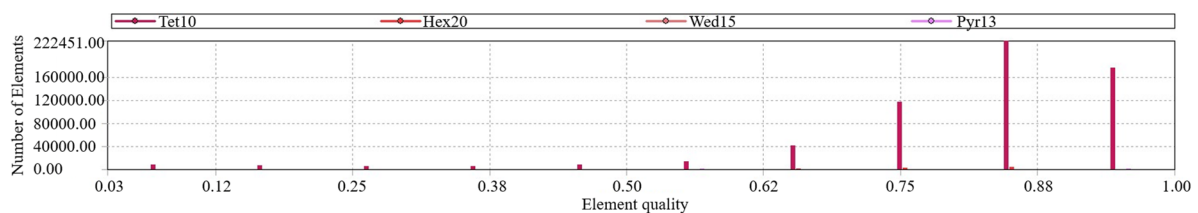


Figure 3. Distribution of element quality for the finite element mesh.

3.2. Location of Maximum Stress and Strain

As illustrated in Figure 4a,b, the maximum equivalent von Mises stress and equivalent elastic strain are concentrated within the copper heat spreader region. This identifies the heat spreader as the primary structural component bearing thermo-mechanical deformation during thermal loading. Specifically, these peaks occur near the sidewall edges directly above the TOTV array.

This localized concentration is attributed to:

1. Thermal Expansion Mismatch: Significant CTE differences between the copper heat spreader, the surrounding SiO₂ dielectric, and the silicon substrate.
2. Geometrical Discontinuities: Localized stiffness variations at the interfaces between the TOTVs and the heat spreader.

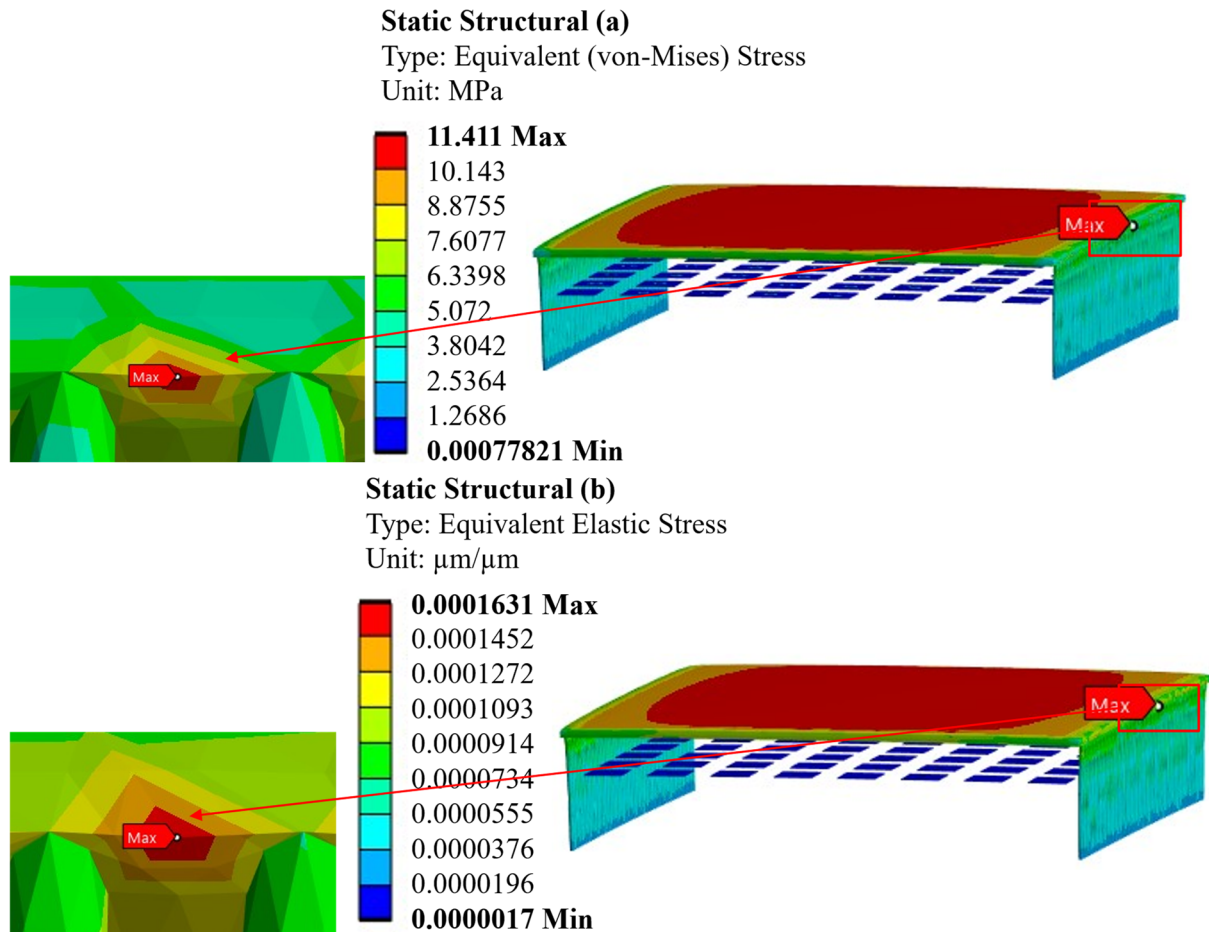


Figure 4. Distributions of (a) equivalent von Mises stress and (b) equivalent elastic strain in the TOTV structure under thermal loading.

3.3. Single-Objective Optimization

3.3.1. Optimization of Stress and Strain

Under the initial configuration, the maximum stress and strain occur at the bottom surface of the copper heat spreader near geometric transitions. This behavior is driven by thermal expansion mismatch and resulting bending deformations. The mechanical constraints of the underlying layers force the heat spreader to bend, concentrating stress at its lower interface. Comparison of the design cases is summarized in Table 3.

Table 3. Comparison of simulation and verification results of the five design cases.

Design Case	D (μm)	Pitch	T (nm)	Maximum Equivalent von Mises Stress (MPa)		Maximum Equivalent Elastic Strain		Energy Consumption (fJ)	Compared with the Original Design
				Optimization	Verification	Optimization	Verification		
1	0.30	48	400	11.411	-	0.0001631	-	7.4355	-
2	0.42	41	672	10.392	10.651	0.0001446	0.0001426	14.682	Minimize equivalent stress
3	0.50	36	660	10.864	10.831	0.0001367	0.0001353	19.915	Minimize equivalent strain
4	0.30	4	1000	15.227	15.264	0.0002168	0.0002181	7.323	Minimize energy consumption
5	0.30	40	656	11.199	11.147	0.0001557	0.0001655	7.406	RSM combined with MOGA

As shown in Table. 3, in this study, the original design is defined as Design Case 1, exhibiting a maximum equivalent stress of 11.411 MPa and a maximum equivalent strain of 0.0001631.

In the stress-oriented single-objective optimization (Case 2), the optimal design parameters are identified as a TOTV diameter of 0.21 μm , TOTV count of 41 (corresponding to a smaller pitch), and a heat spreader thickness of 672.95 nm. Under this configuration, the maximum von Mises stress is reduced from 11.411 MPa in the original design (Case 1) to 10.392 MPa shown in Figure 5, achieving an improvement of approximately 9%. Validation simulations yielded 10.651 MPa, with a prediction error of only 2.4%.

In the strain-oriented single-objective optimization (Case 3), the optimal parameters are determined as a TOTV diameter of 0.25 μm , a TOTV count of 36, and a heat spreader thickness of 660 nm. Under these conditions, the maximum equivalent strain is reduced from 0.0001631 in the original design (Case 1) to 0.0001367, corresponding to an improvement of approximately 16%. Validation results yielded a maximum strain of 0.0001353 and showed a negligible 1% discrepancy between predicted and simulated values.

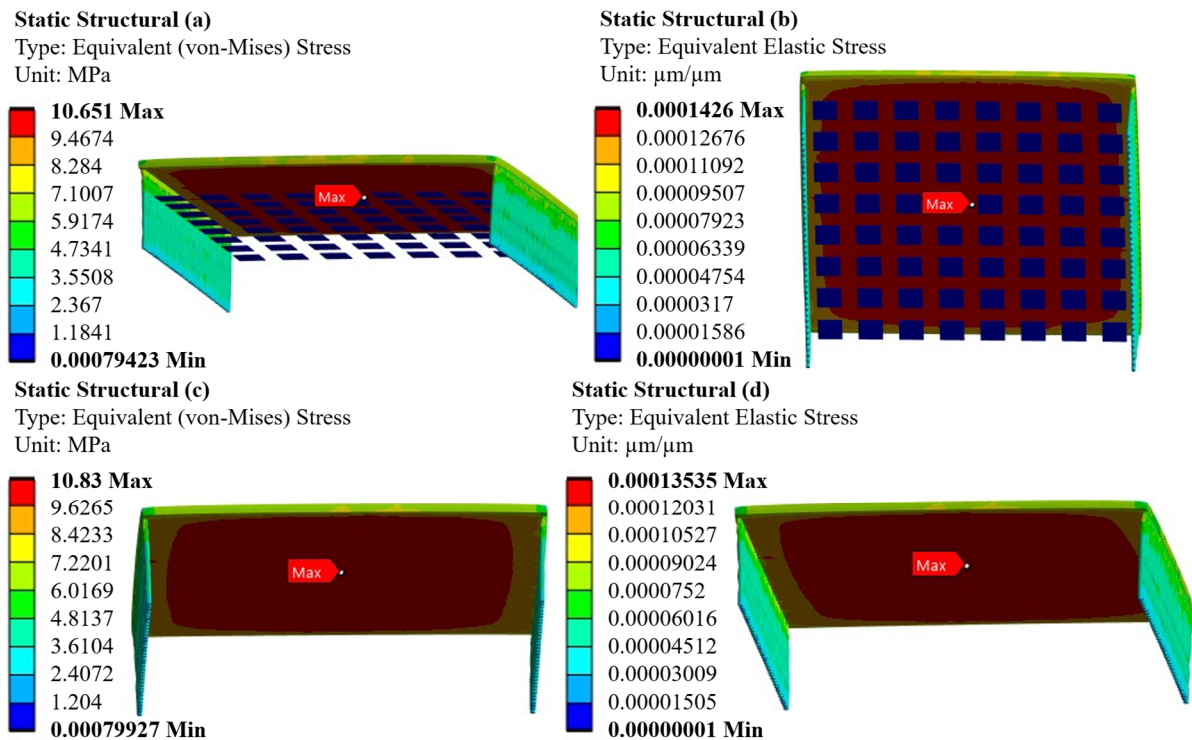


Figure 5. Validation results of the optimization. (a) maximum equivalent stress distribution for case 2; (b) maximum equivalent elastic strain distribution for case 2; (c) Scheme 3 maximum equivalent stress distribution; (d) Scheme 3 maximum equivalent elastic strain distribution.

As illustrated by the response surface plots in Figure 6a,b, the effects of the three design variables on stress exhibit a concave trend, indicating the presence of an optimal combination that minimizes stress. Notably, increasing the TOTV count (i.e., reducing pitch) leads to a more pronounced reduction in stress. As shown in Figure 6c,d, the response surfaces for strain also exhibit a concave profile, although the dominant trends differ from those of stress.

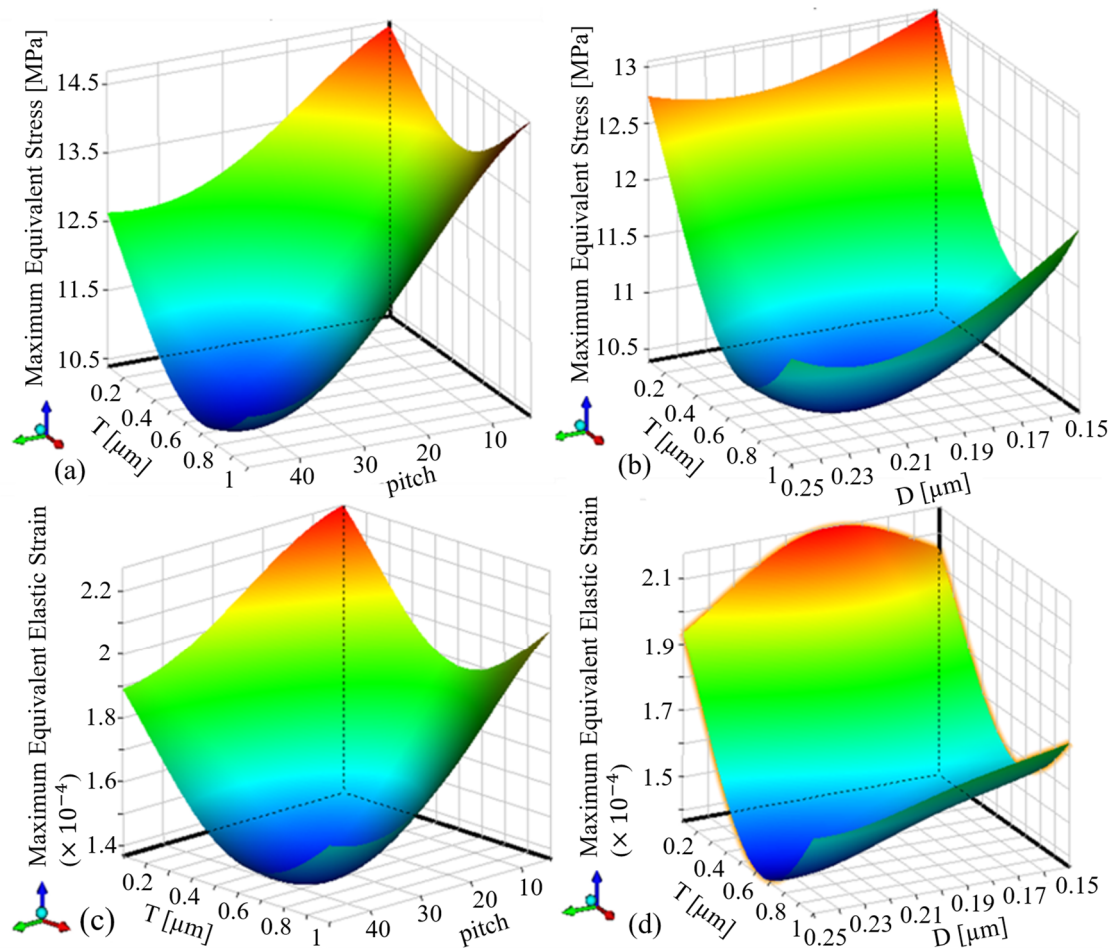


Figure 6. Three-dimensional response surfaces showing the interaction effects of geometric parameters: maximum equivalent stress is mapped against (a) T vs. pitch and (b) T vs. D; maximum equivalent elastic strain is mapped against (c) T vs. pitch and (d) T vs. D.

According to the sensitivity analysis in Figure 7a, the TOTV count is the most influential parameter affecting stress, followed by the heat spreader thickness, while the TOTV diameter has the least impact. Figure 7b reveals that the heat spreader thickness is the most influential parameter governing strain, followed by the TOTV count, while the TOTV diameter plays a relatively minor role.

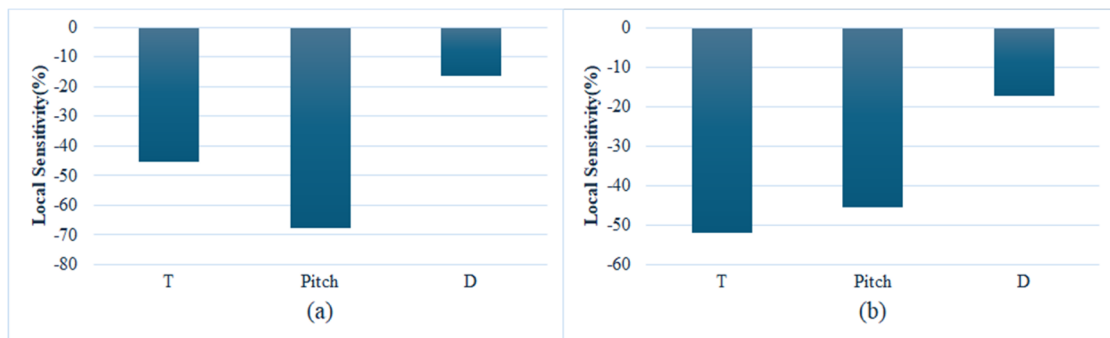


Figure 7. Parameter sensitivity results for (a) maximum equivalent stress and (b) maximum equivalent elastic strain within the TOTV structure.

3.3.2. Optimization of Energy Consumption

In the single-objective optimization for energy consumption, the total capacitance C_{tot} is adopted as the energy-related performance metric, as defined earlier. Since the energy consumption is directly proportional to the total capacitance, minimizing C_{tot} effectively represents the reduction of energy dissipation. Figure 8 presents the parameter sensitivity analysis of the capacitance-based energy metric. It is observed that the sensitivity trend of the

total capacitance closely follows that of the self-capacitance C_{self} , indicating that self-capacitance dominates the overall capacitive behavior. This dominance can be explained by the magnitude comparison among the capacitance components: under the geometric scales considered in this study, the self-capacitance exhibits a significantly larger numerical magnitude than both the mutual and plane capacitances, thereby governing the total capacitance.

This behavior can be physically explained by the geometric dependence of self-capacitance, which scales directly with the via cross-sectional area. Consequently, reductions in TOTV diameter lead to a substantial decrease in self-capacitance and thus total energy consumption. In contrast, mechanical optimization strategies tend to favor increased via density, larger diameters, and thicker heat spreaders to suppress stress and strain, all of which inherently enlarge capacitive coupling areas. As a result, mechanically optimized designs inevitably incur higher electrical energy penalties.

Further inspection of the sensitivity results reveals that the self-capacitance is primarily controlled by the TOTV diameter, which is its sole geometric variable. Consequently, the total capacitance shows the highest sensitivity to variations in diameter. Although the mutual capacitance depends on the spacing between adjacent TOTVs, its overall contribution remains secondary. The plane capacitance, on the other hand, is mainly influenced by the heat spreader thickness, and this effect is reflected in the corresponding sensitivity results, but it does not dominate the total energy behavior.

A quantitative comparison of energy performance among the four design schemes is summarized in Table 2. Although the energy-optimal design (Case 4) exhibits only a modest reduction of approximately 1.5% compared with the original design (Case 1), its advantage becomes more evident when compared with the mechanically optimized solutions. Specifically, the energy consumption of Case 4 is reduced by approximately 50% relative to the stress-optimal design (Case 2) and by 63% relative to the strain-optimal design (Case 3). These results clearly indicate that designs optimized solely for mechanical reliability may lead to substantially higher energy penalties.

Overall, the single-objective energy optimization demonstrates that reducing the TOTV diameter is an effective approach to suppress self-capacitance and thereby lower total energy consumption.

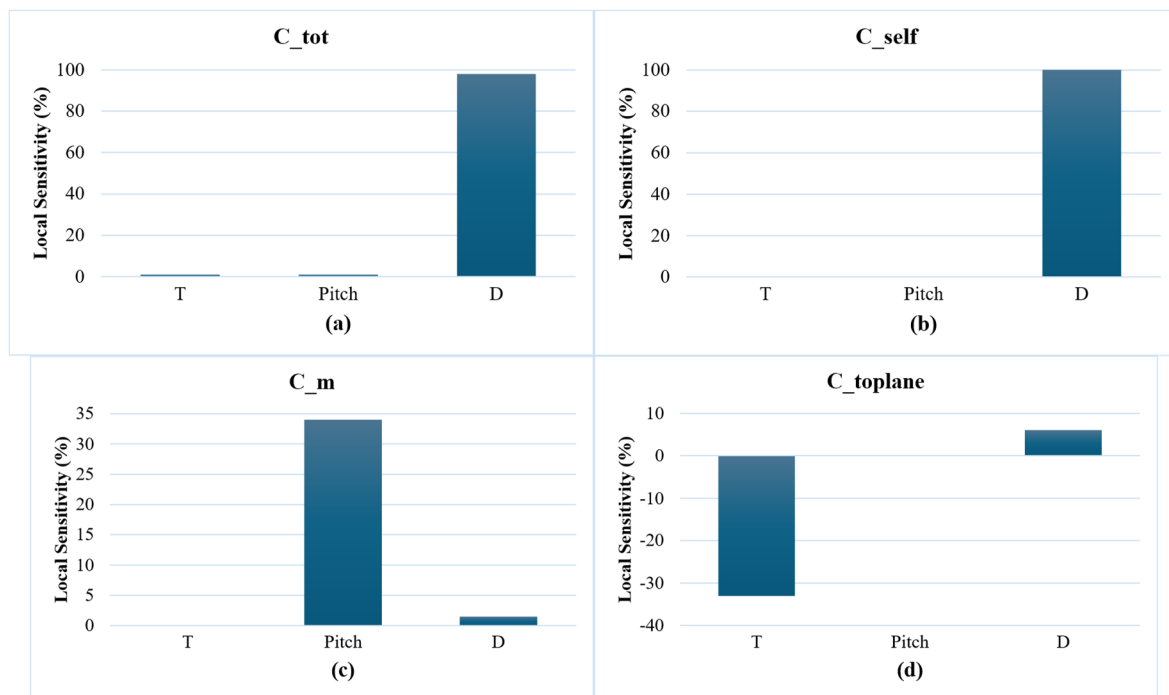


Figure 8. Local sensitivity analysis of geometric parameters regarding electrical performance metrics: (a) total effective capacitance (C_{tot}), (b) self-capacitance (C_{self}), (c) mutual capacitance (C_m), (d) TOTV-to-plane capacitance (C_{tp}).

3.4. Weighted Multi-Objective Optimization

To further investigate the trade-off between mechanical reliability and electrical performance, a weighted multi-objective optimization was conducted. In this formulation, the normalized mechanical metrics, including the maximum equivalent stress and maximum equivalent strain, were combined with electrical metrics, namely equivalent resistance and mutual capacitance, through different weighting ratios to represent distinct design preferences.

Figure 9 illustrates the local sensitivity of the design variables under mechanical weighting factors of 50%, 60%, and 70%. As the mechanical weighting increases, the thickness of the heat spreader *T* exhibits a progressively stronger negative sensitivity, indicating an increasing tendency toward thicker structures to suppress stress and strain concentrations. In contrast, the TOTV pitch consistently shows positive sensitivity across all weighting conditions, reflecting its coupled influence on both mechanical and electrical responses. The effect of the TOTV diameter remains comparatively minor, suggesting a secondary role within the explored design range.

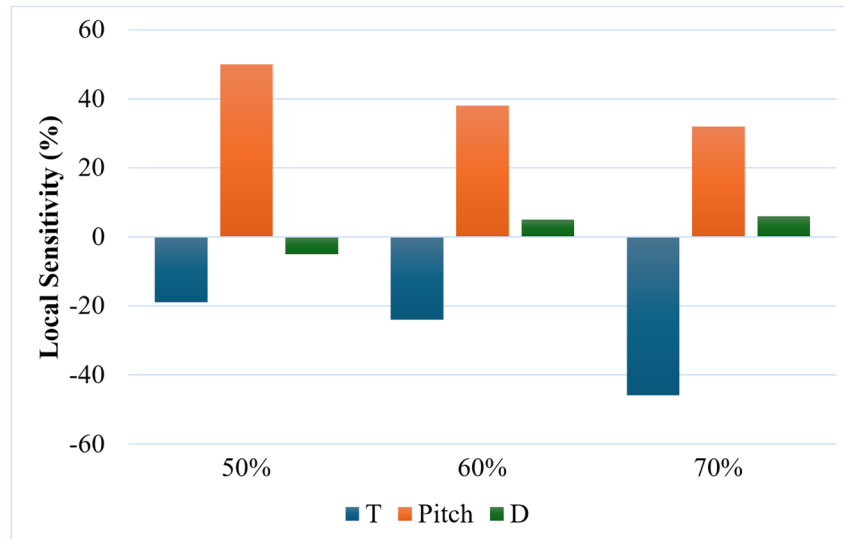


Figure 9. Local sensitivity analysis of design variables across varying mechanical weighting factors (50%, 60%, and 70%) within the multi-objective optimization framework.

Table 4 summarizes the optimal design parameters and corresponding performance metrics obtained under different weighting ratios. As the mechanical weighting increases from 50% to 70%, the maximum equivalent von Mises stress decreases from 12.739 MPa to 11.066 MPa, while the maximum equivalent elastic strain is reduced from 0.00017333 to 0.00015146, demonstrating a clear improvement in thermo-mechanical reliability. However, this improvement is accompanied by a gradual degradation in electrical performance metrics, highlighting the inherent trade-off between mechanical robustness and electrical efficiency.

Based on this comparison, a mechanical weighting factor of 60% was selected as a representative balanced design preference. This weighting provides a noticeable reduction in stress and strain while avoiding excessive penalties in electrical performance, thereby offering a practical compromise suitable for reliability-oriented TOTV structural design.

Table 4. Optimal design parameters and corresponding mechanical and electrical performance under different mechanical–electrical weighting ratios.

Weighting Ratio	D (μm)	Pitch	T (nm)	Maximum Equivalent von Mises Stress (MPa)	Maximum Equivalent Elastic Strain	C _m (fF)	R _{eq} (Ω)	E (fJ)
50%	0.21614	12	635	12.739	0.00017333	0.03045	0.0881	15.223
60%	0.20420	22	656	11.581	0.00015948	0.05971	0.0537	13.621
70%	0.20767	27	663	11.066	0.00015146	0.08081	0.0423	14.106

Conversely, the electrical performance shows an opposite trend. With increasing mechanical weight, the mutual capacitance *C_m* increases, leading to a higher equivalent energy consumption *E* for the 70% weighting case compared to the 60% case. This behavior indicates that excessive emphasis on mechanical reliability may adversely affect electrical efficiency, underscoring the sensitivity of the optimal solution to design preference selection.

It should be emphasized that the weighting ratios adopted in this study are not intended to represent absolute or application-specific priorities. Rather, they are employed to illustrate how optimal design tendencies evolve as the relative importance of mechanical reliability and electrical performance shifts. Among the examined cases, the 60% mechanical weighting is presented as a representative compromise within the explored design space, offering balanced improvements in stress and strain without incurring disproportionate electrical penalties. The Pareto-

front analysis remains the primary global decision-making reference, while the weighted optimization serves as a complementary preference-oriented evaluation tool.

4. Results and Discussion

4.1. Trade-off Behavior in Three-Objective Optimization

In the structural design of TOTV architectures, the maximum equivalent stress, maximum equivalent strain, and energy consumption are adopted as key indicators representing structural reliability, geometric integrity, and electrical efficiency, respectively. These objectives are inherently conflicting, making it impossible to simultaneously achieve their individual theoretical optima. To systematically capture these competing requirements, a three-objective optimization framework was established by integrating response surface approximation with a Multi-Objective Genetic Algorithm (MOGA), enabling exploration of the global design space.

Figure 10 presents the resulting three-dimensional trade-off distribution, where the X-, Y-, and Z-axes correspond to the maximum equivalent stress, maximum equivalent strain, and energy consumption E , respectively. Each point in the Pareto cloud represents a feasible design candidate obtained from finite element simulations. The slanted distribution of solutions clearly indicates that improvements in mechanical performance, such as reductions in stress or strain, are generally accompanied by increased energy consumption. Conversely, designs with lower energy consumption tend to exhibit elevated mechanical responses.

This Pareto distribution quantitatively demonstrates the intrinsic trade-off relationships among the three objectives and confirms that extreme single-objective optimization is insufficient for practical TOTV design. Instead, the Pareto front provides a rational basis for selecting balanced design solutions according to specific performance priorities.

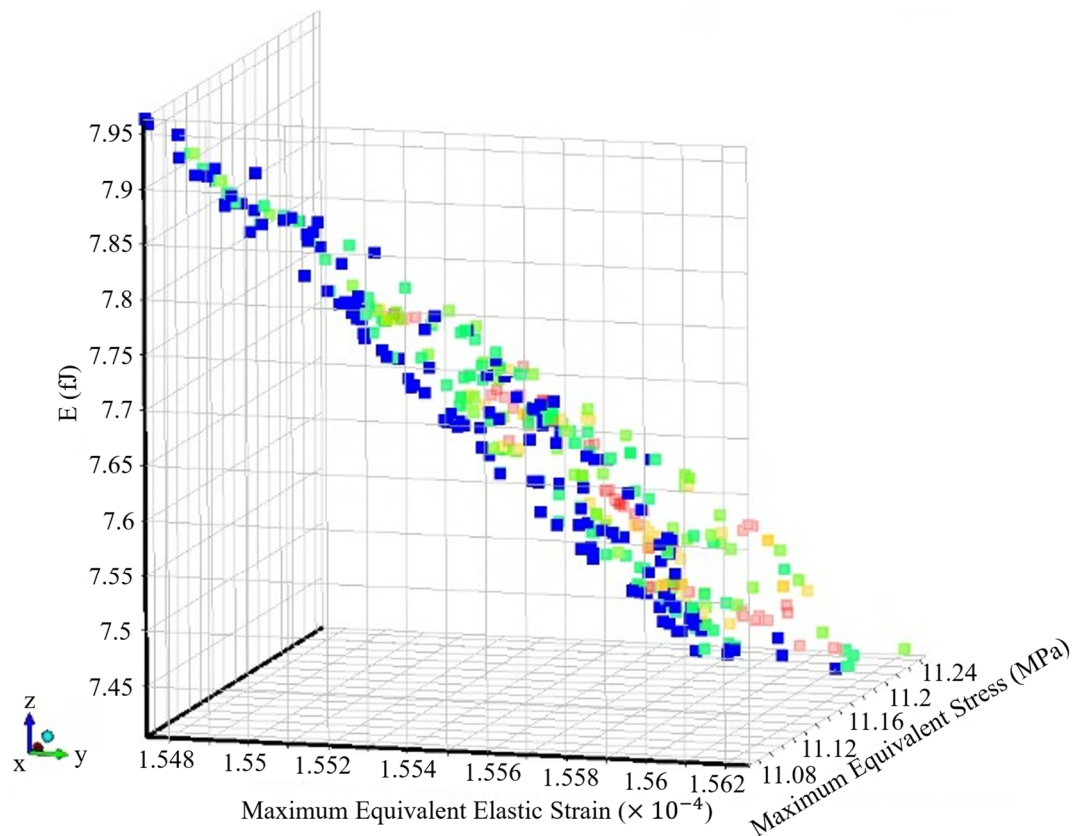


Figure 10. Trade-off diagram and Pareto leading edge of multi-objective optimization results.

4.2. Comparison of Representative Design Cases and Physical Interpretation

To further clarify the practical implications of this three-objective optimization, five representative design cases were selected and summarized in Table 3. Case 1 represents the original design and serves as the baseline for comparison. Case 2 and Case 3 correspond to the single-objective optimal solutions for minimizing equivalent

stress and equivalent strain, respectively. Case 4 is designated as the energy-minimized solution, while Case 5 represents the multi-objective optimal solution that considers stress, strain, and energy consumption simultaneously.

Quantitative analysis in Figure 11 reveals that Case 2 effectively lowers the maximum equivalent stress but results in significantly higher energy consumption compared to the baseline original design. Similarly, Case 3 achieves the lowest equivalent strain but incurs a substantial increase in energy consumption. In contrast, Case 4 successfully minimizes energy consumption but exhibits elevated stress and strain levels, which introduces significant concerns regarding the long-term structural reliability of the package. Among all the examined candidates, Case 5 demonstrates the most balanced and superior performance profile. Compared to the original baseline, Case 5 achieves noticeable reductions in both equivalent stress and strain while maintaining a much lower energy footprint than the single-objective solutions optimized strictly for mechanical reliability. This result emphasizes the distinct advantage of multi-objective optimization in preventing the performance degradation often triggered by extreme single-objective focus.

The response surface plots systematically reveal the non-linear correlations between geometric variables and physical responses, demonstrating that the maximum equivalent stress and strain exhibit distinct concave trends with respect to design parameters such as thickness, pitch, and diameter. These surfaces confirm that physical indicators do not follow simple linear relationships but instead possess local optimal points. Specifically, via pitch (TOTV count) is identified as the dominant factor influencing stress levels, whereas the thickness of the heat spreader shows a higher sensitivity in suppressing structural strain. Such non-linear responses illustrate that a single geometric adjustment can simultaneously impact both structural strength and geometric integrity through complex physical mechanisms.

Further analysis of the 3D trade-off chart reveals the conflicting nature between mechanical reliability and electrical energy efficiency, characterized by the slanted “Pareto Cloud” distribution. Quantitative results indicate that as a design strives to minimize thermal stress and strain for enhanced reliability, it often leads to an increase in parasitic capacitance, which significantly elevates dynamic energy consumption—in some cases by up to 63% during single-objective optimization. The Pareto Leading Edge defines the physical limits of achievable performance without sacrificing one metric for another. The selected Case 5 is positioned precisely on this balanced frontier, proving that a multi-objective optimization framework is essential for identifying “energy-aware” solutions within the constraints of structural and electrical trade-offs.

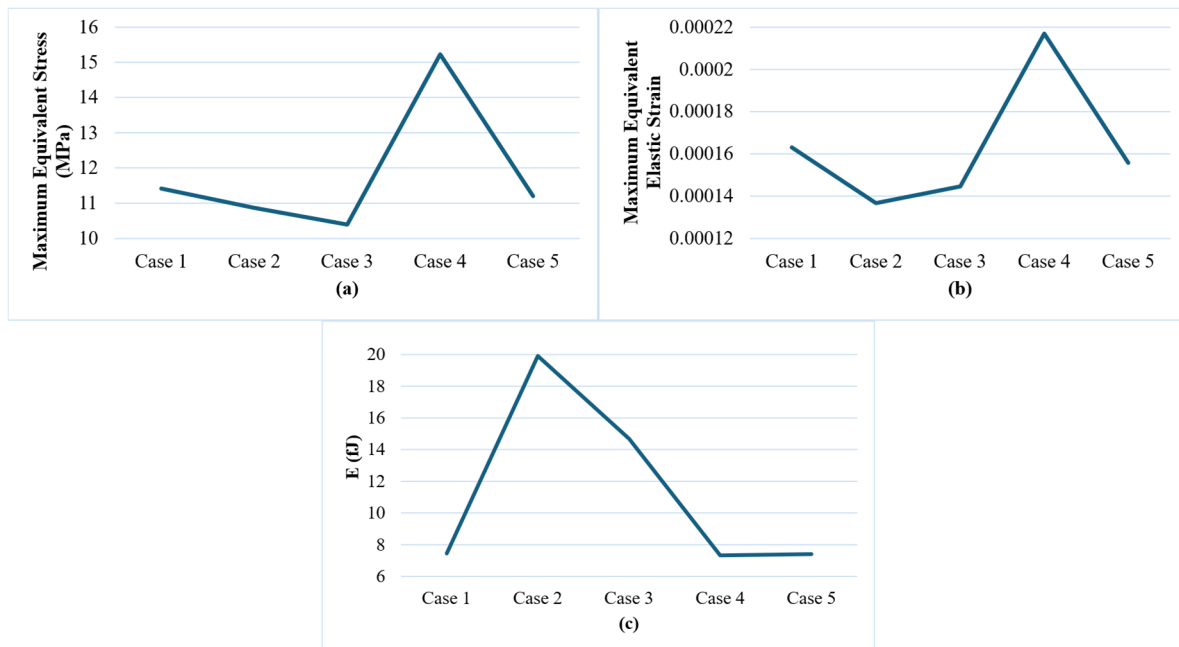


Figure 11. Comparison of (a) maximum equivalent von Mises stress, (b) maximum equivalent elastic strain, and (c) energy consumption for the five representative design cases.

4.3. Quantitative Comparison and Selection of the Optimal Design

To quantitatively justify the selection of Case 5 as the final optimal design, a comparative performance assessment was conducted against other representative design candidates using the data summarized in Figure 11. This analysis aims to clarify the specific trade-offs and performance gains achieved through the proposed multi-objective optimization framework.

First, when compared with Case 2 (the stress-optimal design), Case 5 exhibits a moderate increase in maximum equivalent stress of approximately 7%. However, this minor mechanical compromise is accompanied by a substantial 62.8% reduction in energy consumption. This result indicates that a slight relaxation of peak stress constraints can lead to a pronounced improvement in electrical energy efficiency at the system level.

Similarly, relative to Case 3 (the strain-optimal design), Case 5 shows an increase of approximately 12% in maximum equivalent elastic strain. In return, the total energy consumption is reduced by 49.5%. This comparison further demonstrates that accepting limited additional deformation can yield significant power-saving benefits, validating the effectiveness of the multi-objective optimization strategy in balancing competing objectives.

In contrast, when compared with Case 4 (the energy-optimal design), Case 5 incurs only a negligible 1.1% increase in energy consumption. Despite this nearly identical electrical performance, Case 5 achieves a 26.4% reduction in equivalent stress and a 28.2% reduction in equivalent strain. These results highlight that Case 5 substantially enhances structural reliability and geometric stability while maintaining almost the same energy efficiency as the purely energy-driven design.

Overall, Case 5 consistently avoids the extreme compromises observed in single-objective optimization cases. It provides a well-balanced solution that simultaneously achieves satisfactory mechanical reliability and high electrical energy efficiency. Therefore, Case 5 is formally selected as the optimal design, representing the successful outcome of the proposed multi-objective optimization framework for advanced TOTV structures.

Although the present study focuses on thermo-mechanical and electrical optimization of TOTV structures for 3D integrated circuits, the obtained results provide important implications for silicon photonics integration. In silicon photonic platforms, localized temperature gradients and thermally induced mechanical deformation are known to cause refractive index drift, optical phase instability, and potential misalignment of optical interconnect components. Therefore, suppressing thermal stress concentration and deformation is essential for maintaining stable photonic device performance.

The optimized TOTV configurations obtained in this work exhibit significantly reduced peak stress and strain in the heat spreader and surrounding dielectric regions. This improvement indicates a more uniform thermal expansion behavior and mitigated local deformation near interconnect interfaces. From a silicon photonics perspective, such thermo-mechanical stabilization is beneficial for minimizing optical path-length variation and preserving alignment between optical waveguides and vertical interconnect structures. Although optical performance is not explicitly simulated in this study, the demonstrated reduction of thermo-mechanical disturbance suggests that the proposed TOTV optimization framework provides a physically consistent foundation for future thermally stable and energy-aware silicon photonic packaging design [8].

It is instructive to compare the proposed TOTV architecture with conventional TSV-based interconnects. In standard TSV structures, copper vias primarily serve as electrical signal transmission paths embedded directly within silicon substrates. As a result, TSV arrays often introduce strong thermo-mechanical stress inside the silicon due to the large CTE mismatch between copper and silicon. Furthermore, dense TSV arrays lead to considerable parasitic capacitance and electrical energy dissipation, directly impacting signal integrity and power efficiency.

In contrast, the TOTV structure investigated in this study is embedded within a dielectric oxide layer and primarily functions as a vertical thermal conduction path connected to a heat spreader. This configuration fundamentally alters both mechanical and electrical behaviors. Mechanically, embedding vias in oxide redistributes stress away from active silicon regions and shifts stress concentration toward the heat spreader–oxide interface, reducing the risk of silicon cracking or device-layer deformation. Electrically, since TOTVs are not employed as high-speed signal interconnects, their parasitic capacitance mainly contributes to energy consumption rather than signal degradation. This allows TOTV geometries to be optimized specifically for thermal management and mechanical reliability while controlling electrical energy penalties.

The optimization results show that increasing TOTV count and heat spreader thickness effectively suppress thermo-mechanical stress, whereas reducing TOTV diameter primarily lowers capacitive energy consumption. These optimization trends differ from conventional TSV design, where signal integrity constraints dominate geometric selection. Therefore, the proposed TOTV design framework provides a complementary interconnect strategy to traditional TSV architectures, particularly suitable for thermally critical and energy-sensitive 3D heterogeneous integration and silicon photonics packaging platforms [7].

5. Conclusions

This study employed three-dimensional finite element analysis (FEA) to investigate the coupled thermo-mechanical behavior and electrical energy performance of Through-Oxide Thermal Via (TOTV) structures under thermal cycling conditions. A robust 3D numerical model was established and validated through mesh

convergence analysis and qualitative consistency with trends reported in prior literature. Within the present modeling framework, single-objective optimization results indicate that copper thickness and via radius are dominant geometric parameters governing thermo-mechanical response, with peak stress reductions on the order of 18.3% observed relative to the baseline design.

A key finding of this work is that aggressive optimization targeting a single performance metric may induce substantial penalties in competing objectives. In particular, mechanically optimized configurations were found to increase electrical energy consumption by up to 63% compared with energy-oriented designs, highlighting the strong coupling between structural reliability and parasitic-driven electrical behavior. These quantitative results are not intended as absolute performance predictions, but rather as indicators of the relative magnitude of trade-offs under consistent geometric assumptions and boundary conditions.

By employing a Multi-Objective Genetic Algorithm (MOGA), the study systematically quantified these competing trends and identified a Pareto-optimal design set. Within this set, a representative balanced configuration (Case 5) achieved a reduction of approximately 14.8% in maximum principal stress and up to 72% reduction in axial deformation relative to the original design, while avoiding excessive degradation in electrical energy efficiency. These improvements reflect the effectiveness of compromise-based optimization rather than extreme single-metric optimization.

Overall, this work demonstrates that integrating three-dimensional FEA with multi-objective optimization enables a physically consistent evaluation of trade-offs between thermo-mechanical reliability and electrical energy behavior in TOTV structures. The proposed framework is best suited as an early-stage design-space exploration and decision-support tool, providing quantitatively grounded insight into relative performance trends. Owing to the use of simplified electrical models, fixed via-length assumptions, and the absence of experimental validation, the reported numerical values should be interpreted as comparative indicators rather than definitive design targets. Future work incorporating experimental benchmarking and high-fidelity electromagnetic simulations would further strengthen predictive capability.

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