Review

Applications of Graphene in Post-Moore Electronic Devices

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Abstract: As Moore's Law approaches its physical and economic limits, the pursuit of alternative electronic paradigms has become critical. Graphene, a one-atom-thick material with exceptional electrical, thermal, and mechanical properties, offers promising opportunities for next-generation devices in the post-Moore era. This perspective article explores graphene's role in three key computing frontiers: (1) beyond-CMOS transistors, where its high carrier mobility and atomic thinness support ultra-fast, scaled devices; (2) neuromorphic computing, where graphene-based synaptic devices exhibit energy-efficient, analog learning behaviors; and (3) quantum technologies, where graphene enables tunable superconducting junctions, spin qubits, and moiré-based correlated states. We highlight the fundamental physics underlying these applications, survey the recent engineering advances, and assess the major challenges—such as bandgap engineering, device variability, and large-scale integration. Through careful material design and heterogeneous integration, graphene is poised to become a critical enabler of hybrid electronic architectures that extend the capabilities of conventional silicon and help usher in a new era of information processing.

Keywords: graphene; post-Moore; beyond-CMOS; transistors; neuromorphic computing; quantum devices

1. Introduction

For decades, the microelectronics industry followed *Moore's Law*, relentlessly scaling down silicon transistor dimensions to pack more devices into integrated circuits [1]. This scaling produced exponential improvements in computing performance and energy-efficiency. However, as silicon transistors approach fundamental limits of size and leakage, traditional scaling is faltering. Chipmakers have already resorted to innovations like three-dimensional FinFET transistors, new materials (high-*k* dielectrics, metal gates), and chip stacking to sustain progress. Yet, even these measures cannot continue indefinitely. The *post-Moore era* refers to the coming age when boosting computational power will require novel paradigms beyond simply shrinking conventional silicon CMOS devices.

In this context, graphene–a one-atom-thick sheet of carbon with exceptional electronic properties–has emerged as a promising material to extend or augment silicon technologies [2]. Graphene offers extremely high carrier mobility, high current-carrying capacity, flexibility, and atomic thickness, all of which could be advantageous in future electronic devices (Table 1). Researchers envision integrating graphene into next-generation transistors, neuromorphic computing architectures, and quantum devices as a way to bypass the limits of silicon CMOS. Such integration must be compatible with existing silicon platforms, leveraging graphene's unique attributes without requiring a complete replacement of the established CMOS infrastructure.

However, graphene is not a panacea. It lacks a natural bandgap, making it difficult to turn off in digital logic applications [3]. Moreover, incorporating atomically thin graphene into complex circuits poses challenges in fabrication, uniformity, and interfacing with other materials [4,5]. Nevertheless, its potential to enable new device concepts–from high-frequency transistors to synaptic electronics and quantum components–is driving intense research. This article provides a broad overview of graphene's applications in three key post-Moore paradigms (Figure 1): (1) Transistors beyond traditional CMOS; (2) Neuromorphic computing devices inspired by the brain;

(3) Quantum devices for next-generation computing. A detailed comparison of the performance of the three paradigms is shown in Table 2. In each domain, we highlight the fundamental science behind graphene's role, the engineering achievements to date, and the remaining challenges that must be overcome to realize graphene-enabled computing in the post-Moore era. Through this integrated analysis, we aim to provide researchers and industry stakeholders with a fundamental understanding of graphene's unique capabilities.

Table 1. Comparative analysis of key performance metrics between graphene and silicon.

Properties	Graphene	Silicon
Carrier mobility	Up to 200,000 $cm^2/(V·s)$	~1400 $cm^2/(V·s)$
Theoretical strength	130 GPa	~1 GPa
Thermal conductivity	5000 W/(m·K) (monolayer)	~150 W/(m·K)
Current density	$>10^9$ A/cm^2	~10^5 A/cm^2
Optical transparency	97% (monolayer)	Opaque
Flexibility	Fracture strain 20–25%	Brittle (fracture strain < 1%)
Thickness limit	Single atom	Micron-scale

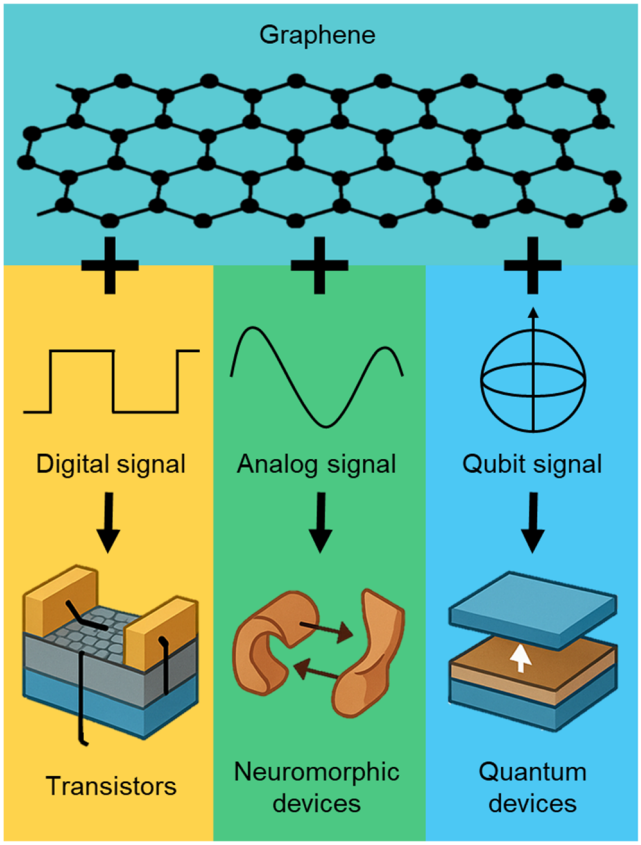

Figure 1. Graphene-based devices for digital, analog, and qubit signal processing in post-Moore era.

Table 2. Key parameter comparison (transistors vs. neuromorphic vs. quantum devices).

Paradigms	Transistors	Neuromorphic Computing	Quantum Devices
Energy efficiency	~1 pJ/operation	0.01–1 fJ/event	High
Speed	ns-scale	μs-scale	ns-scale
Scalability	Moore's law slowing	High (brain-like parallelism)	Exponential qubit growth
Compute paradigm	Boolean logic	Neural networks	Quantum superposition/entanglement
Best-fit applications	General-purpose computing	Spatiotemporal pattern recognition	Quantum algorithms
Thermal management	Active cooling required	Room-temperature operation	Near-absolute-zero cooling

2. Graphene in Transistors Beyond CMOS

As silicon transistors reach their scaling limits, graphene has been investigated as an alternative channel material for future high-performance transistors. Graphene's appeal lies in its extraordinary charge transport–room-temperature carrier mobilities can exceed 10^4–10^5 $cm^2/V{\cdot}s$, far above silicon, potentially enabling faster switching and higher frequency operation [1]. Graphene is also only one atom thick, which means it can form an extremely scaled channel and might be the ultimate limit for thinning down transistors. These properties prompted early optimism that graphene could extend Moore's Law by replacing or augmenting silicon in logic transistors. In fact, around 2010–2011, researchers speculated that graphene might be used in the "next generation of high-performance devices" as silicon's performance gains through scaling leveled off.

High-Frequency and Analog Applications. One area where graphene transistors have already made a mark is in high-frequency (RF) and analog electronics (Figure 2a,b). Even though graphene lacks a bandgap (more on that challenge below), a transistor that need not switch fully off can still amplify AC signals. Graphene field-effect transistors (GFETs) have demonstrated impressive cutoff frequencies (f_T) well into the hundreds of gigahertz, thanks to graphene's high mobility and negligible charge scattering [4]. For example, GFETs with gate lengths on the order of 100 nm have shown $f_T > 400$ GHz in research settings [6]. Such high f_T values approach those of the best III-V semiconductor transistors. The potential for low-noise, high-speed operation makes graphene attractive for analog RF amplifiers, mixers, and terahertz devices in the post-Moore era. The graphene-based radio-frequency receiver IC integrated multiple GFET amplifiers and mixers on a silicon wafer. The graphene IC successfully down-converted a 4.3 GHz wireless signal, highlighting that complex graphene circuits can be built in a CMOS-compatible way. This achievement required careful fabrication to preserve graphene's excellent transport properties–for instance, using techniques that avoid contaminating or damaging the one-atom-thick channels. The result was "unprecedented graphene circuit complexity" integrated on an 8-inch wafer, indicating that graphene devices can potentially be scaled and manufactured alongside silicon, at least for analog electronics.

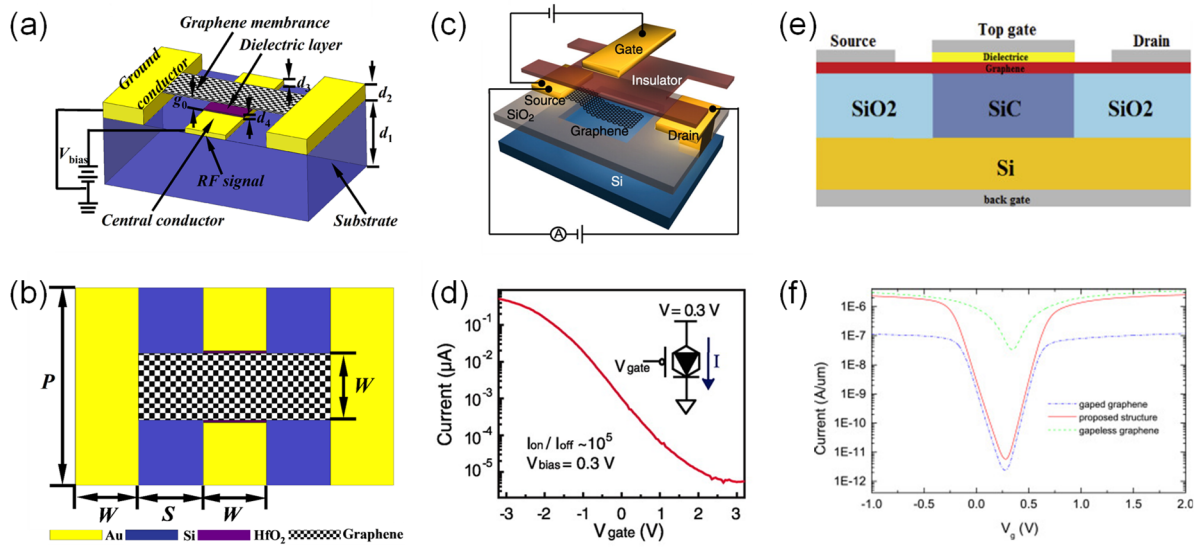

Figure 2. Graphene in transistors beyond CMOS. Schematic illustration of the graphene RF NEMS capacitive switch: (**a**) isometric 3D view; (**b**) top-down view [7]. (**c**) Schematic illustration of the graphene barrister [8]. (**d**) Forward diode current versus gate voltage in the graphene barrister at V_{bias} = 0.3 V [8]. (**e**) Schematic illustration of graphene tunnelling field effect transistor [9]. (**f**) Drain current versus gate voltage for graphene TFETs at V_{ds} = 0.1 V [9].

The Bandgap Challenge for Digital Logic. Despite these successes in analog domains, graphene has a fundamental limitation for digital logic applications: it is a gapless semimetal. In a conventional silicon CMOS transistor, the silicon channel has a bandgap (~1.1 eV for Si) that allows the device to switch off–yielding a low leakage off-current–and to achieve a high on/off current ratio when gated. Graphene's band structure, by contrast, has no gap; its conduction and valence bands meet at the Dirac point [10]. As a result, a graphene FET cannot be fully turned off–it always conducts some residual current even at zero gate bias. Early experiments found graphene transistors to have on/off current ratios of at best ~5–10 at room temperature, compared to ratios of 10^4–10^7 in modern silicon logic transistors [1]. The inherent leakage makes it difficult to use graphene as a direct drop-in

replacement for CMOS logic, where extremely low off-currents are required for power efficiency and noise margins.

Researchers have pursued several strategies to overcome graphene's lack of a bandgap. One approach is to engineer a bandgap by nanostructuring or chemical modification. For instance, cutting graphene into narrow nanoribbons (width ~10 nm or less) induces quantum confinement that can open a moderate bandgap (several hundred meV) depending on the ribbon width and edge structure. Graphene nanoribbon transistors have shown improved on/off ratios, but fabricating ribbons with uniform, atomically smooth edges at scale remains an enormous challenge–edge defects and line-edge roughness tend to degrade their performance. Another method is to use bilayer graphene: two stacked graphene layers can be made to exhibit a tunable bandgap (up to ~0.1–0.3 eV) when a perpendicular electric field is applied (by using a dual-gate configuration). Bilayer graphene FETs do attain small bandgaps, but the gap is still much smaller than silicon's, and the on/off ratio (perhaps 10^2–10^3 at low temperature for the largest gaps) often falls short for room-temperature logic. Moreover, introducing a bandgap typically comes at the cost of reducing mobility, diminishing one of graphene's primary advantages.

Rather than forcing graphene into a role for which it is ill-suited (a switch that fully turns off), a compelling alternative is to exploit graphene's strengths in novel device concepts that do not require a strict off-state. One such concept is the graphene barristor–a term coined for a graphene-based Schottky barrier transistor. In a barristor, graphene is used as an electrode forming a Schottky junction with a semiconductor (such as silicon or a 2D semiconductor like MoS_2). The transistor action comes from modulating the Schottky barrier height via the graphene electrode's work function (tunable by gate voltage). In 2012, researchers at Samsung demonstrated a graphene barristor with an on/off ratio over 10^5 (Figure 2c,d), effectively using graphene's Fermi level tunability to overcome its lack of a gap [8]. The device exploits graphene's work function modulation to switch current flow from a silicon channel, achieving performance suitable for logic. This clever design showed that graphene can be used in hybrid structures to achieve switching, even if pure graphene alone doesn't switch off.

Another class of graphene-enabled transistor is the tunnel field-effect transistor (TFET). In a tunnel FET, the device is designed such that current arises from quantum tunneling through a barrier, rather than thermionic emission over a barrier as in a conventional FET [1,2]. Graphene's atomically thin nature makes it ideal for tunneling structures–for example, a vertical stack where graphene serves as one electrode and a monolayer semiconductor or insulator forms the tunnel barrier (Figure 2e,f). Extremely short (sub-nanometer) channel lengths can be realized in vertical graphene heterostructure transistors. Researchers have built graphene-based TFETs and vertical graphene transistors that achieve steep switching by quantum tunneling. In one design, graphene was used as a thin electrode in a vertical phase-change memory cell, enabling a selector device with high on/off ratio for memory applications. In another approach, a graphene/MoS_2 heterostructure was used to create a tunneling device where graphene's zero-gap band structure provided a reservoir of carriers that tunnel into the semiconductor's bandgap states under bias, achieving subthreshold swings beyond the CMOS limit.

Graphene has also been explored in reconfigurable transistors–devices that can dynamically switch between n-type and p-type operation. Owing to its symmetrical band structure for electrons and holes (ambipolar conduction), a single graphene transistor can be electrostatically programmed to conduct either electrons or holes depending on gate biases. Such reconfigurable graphene FETs have been demonstrated, hinting at adaptive logic circuits where one device can play multiple roles. Additionally, graphene quantum dot transistors and single-electron transistors have been investigated for potential beyond-CMOS logic that leverages Coulomb blockade and discrete charge states. While these quantum-effect devices remain far from practical integration, they underline the rich device physics that graphene's low-dimensional structure enables.

Challenges in Graphene Transistors. Despite promising demonstrations, graphene transistors face fundamental hurdles that limit their practical adoption. The most significant challenge is about interfacial engineering. Any graphene transistor's performance is highly sensitive to how graphene is integrated with other materials. A major engineering challenge is achieving low-resistance contacts to graphene. Graphene's 2D nature means every atom is at the surface, so contact metals can easily disrupt the carrier flow or induce doping. Considerable research has shown that contact resistances below 200 Ω·μm are achievable with careful choice of metals and contact geometry. Encapsulating graphene with insulating layers like hexagonal boron nitride (hBN) greatly improves its mobility and stability by reducing scattering from surface traps. In laboratory devices, hBN-encapsulated graphene channels with one-dimensional edge contacts have demonstrated near-ballistic transport.

Equally critical is the challenge that scales such techniques to wafer-sized graphene films. Wafer-scale CVD graphene often has grain boundaries and defects that reduce performance relative to small exfoliated flakes. Researchers are actively developing methods to grow graphene at lower temperatures directly on wafers, or to transfer large graphene sheets with minimal damage. For example, integrating graphene and 2D materials monolithically on top of silicon could allow 3D stacking of electronics, where logic, memory, and sensing layers

are built vertically [1]. Such heterogeneous integration could mitigate the end of Moore's Law by adding new functionalities rather than continuing geometry scaling.

Graphene's role in post-Moore transistors is likely to be as an enabler of specialized, high-performance devices rather than a drop-in replacement for silicon CMOS. Graphene can significantly enhance high-frequency analog/RF circuits, where its high conductivity and lack of bandgap are assets. It can also form the basis of novel switching devices (barristors, tunnel FETs, etc.) that circumvent its zero-bandgap limitation by design. Integrating graphene into the silicon platform–for instance, as a back-end-of-line device or a co-planar channel in a 3D stacked transistor–is a key research direction. Continued progress in graphene material quality, fabrication techniques, and interface engineering will determine to what extent graphene transistors can contribute to extending computing performance in the post-Moore era.

3. Graphene in Neuromorphic Computing

As traditional von Neumann computing faces power and parallelism bottlenecks, neuromorphic computing has gained attention as a post-Moore paradigm. Neuromorphic systems draw inspiration from the brain, with networks of "neurons" and "synapses" that process information in parallel and adapt via learning rules. Implementing such brain-like computation in hardware often relies on devices that can mimic the analog, memristive behavior of synapses–for example, gradually changing conductance in response to electrical pulses. Graphene-based materials and devices have shown considerable promise for neuromorphic functions, owing to their mixed electronic-ionic conduction capabilities, stability, and even biocompatibility.

Graphene as a Key to Neuromorphic Transistor Breakthroughs. Overcoming the manufacturing challenges of neuromorphic computing transistors requires embracing the core principles of Moore's Law—continuous innovation, integration density scaling, performance optimization, and cost reduction—while applying them to novel materials, architectures, and 3D integration techniques. Graphene emerges as a transformative enabler, addressing critical hurdles through its ultrahigh carrier mobility, atomic-scale thickness, exceptional gate tunability, ultra-low power potential, and versatility in forming heterostructures. These properties make it an ideal channel material for neuromorphic devices, capable of emulating biological neurons and synapses with high fidelity.

Graphene's electron mobility far surpasses silicon, enabling ultrafast signal propagation essential for real-time neuromorphic processing. Its atomic thinness and electrostatic tunability allow for compact, high-density integration and continuous conductance modulation—key for mimicking synaptic weight changes. Moreover, graphene-based electrolyte-gated transistors can operate at biologically plausible voltages (<1 V), drastically reducing energy consumption. The material's mechanical robustness and flexibility further unlock applications in wearable or implantable neuromorphic systems.

Beyond standalone properties, graphene serves as a platform for van der Waals heterostructures, integrating sensing, memory, and computation into multifunctional devices. This aligns with the Moore's Law ethos of heterogeneous integration while transcending traditional scaling limits. Challenges in CMOS compatibility are being addressed through wafer-scale growth and back-end-of-line integration strategies, positioning graphene as a bridge between conventional silicon and next-generation neuromorphic hardware.

In essence, combining the systematic scaling philosophy of Moore's Law with graphene's unparalleled material advantages offers a compelling path to overcome barriers in neuromorphic transistor fabrication. By leveraging graphene's speed, density, energy efficiency, and design flexibility, future neuromorphic systems can achieve brain-like performance at scale, ushering in a new era of low-power, adaptive computing.

Graphene Memristors and Resistive Memory. One class of neuromorphic devices are *memristors* or resistive random-access memory (RRAM) elements, which can store analog values as conductance states [11–15]. Graphene and its derivatives have been explored in various memristive devices. Graphene oxide (GO), an oxidized form of graphene, is an insulating material that can undergo resistive switching due to the formation/rupture of conductive filaments or reduction/oxidation of functional groups. GO-based memristors have been used to emulate synaptic weights in neuromorphic circuits (Figure 3a,b). For instance, crossbar arrays of graphene oxide devices have been demonstrated for pattern recognition tasks, where the gradual switching of each device's conductance under pulsed voltage mimics synaptic learning rules like spike-timing-dependent plasticity [16]. Graphene itself (conductive) is typically used as electrodes in these structures, while the oxide between acts as the switching medium. One advantage of graphene electrodes is their atomic thickness–when used in vertical RRAM stacks, a monolayer graphene electrode occupies effectively no vertical space, allowing very high-density 3D memory integration. Additionally, graphene's flexibility and chemical inertness can improve the endurance of memristors by accommodating stress and preventing diffusion of metallic species. Researchers have reported multilayer

graphene used as a floating electrode or diffusion barrier in memory cells to enhance retention and reduce crosstalk, pointing to uses in non-volatile memory for neuromorphic systems.

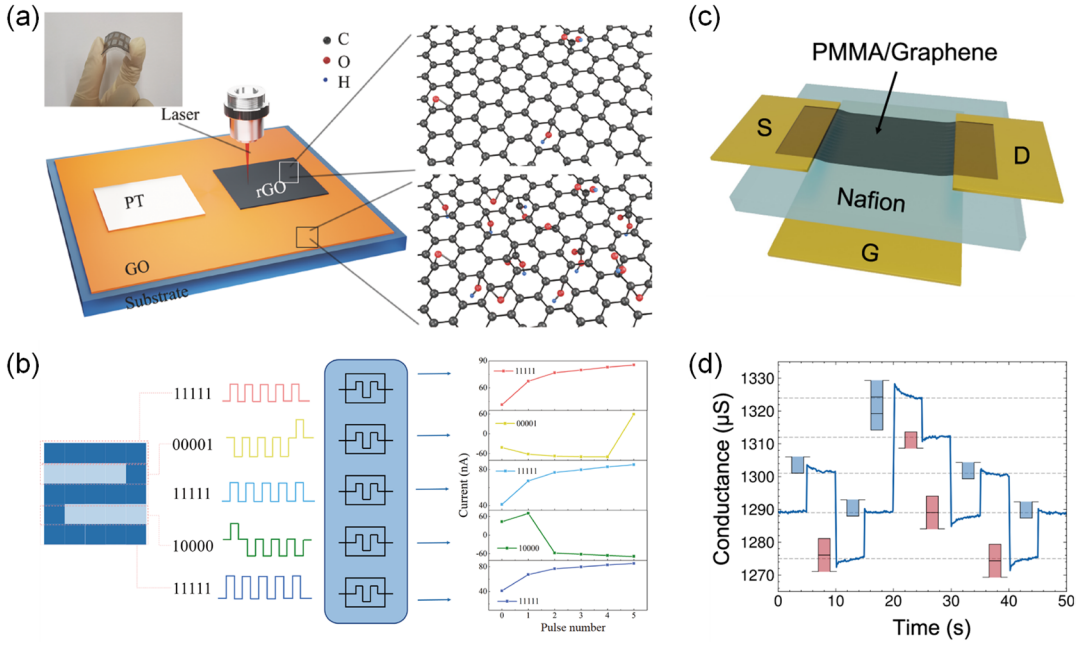

Figure 3. Graphene in neuromorphic computing. (**a**) Schematic illustration of the laser-written Pt/GO/rGO memristor device structure [17]. (**b**) Operation schematic of a Pt/GO/rGO memristor RC system performing number classification [17]. (**c**) 3D schematic illustration showing the S, D, and G electrodes of the BLAST device [13]. (**d**) Time-dependent conductance of BLAST device under periodic gate current pulsing, showing reproducible multi-level states (pulse color/direction indicates polarity; length represents amplitude) [13].

Graphene Synaptic Transistors. Beyond two-terminal memristors, three-terminal synaptic transistors offer another route to emulate synapse-like behaviors. These are typically field-effect transistors where the channel conductance can be gradually adjusted by electrical stimuli, analogous to potentiation or depression of a synapse. Graphene has been employed in such devices in a few different ways. In one approach, graphene is the channel material in an electrochemical transistor: a solid electrolyte (or ion gel) top-gate can inject ions into the graphene, modulating its conductivity. By controlling the ion drift, the conductance of the graphene channel can be incrementally increased or decreased, achieving non-volatile memory of past stimuli. A recent breakthrough in this vein is the development of bilayer graphene artificial synaptic transistors. In 2022, Kireev et al. reported *BLAST* (biocompatible bilayer graphene-based artificial synaptic transistor) devices that use a graphene channel alongside an ion-trapping top layer to achieve highly energy-efficient synaptic behavior (Figure 3c,d) [13]. The BLAST device consists of a two-layer graphene film (to improve conductivity and stability) covered by a thin solid electrolyte (Nafion). Applying a gate voltage drives small ions in the electrolyte to the graphene interface, tuning its conductance. Significantly, these devices achieved switching energy of only ~50 attojoules per μm^2–orders of magnitude lower than previous 2D-material synapses. The ultra-low energy consumption (well below the ~1 fJ per synapse estimated for the human brain) and the ability to support > 10 kHz operation make such graphene synaptic transistors highly attractive for neuromorphic computing. Moreover, the devices exhibited *metaplasticity*—a higher-order form of plasticity akin to biological synapses, meaning their rate of learning itself can adapt. In simulations of neural network learning, these metaplastic graphene synapses actually outperformed ideal linear synapses in accuracy for tasks like image classification. This highlights that beyond mimicking basic synaptic weight updates, graphene devices can capture more complex adaptive behaviors beneficial for AI workloads.

Importantly, graphene and its derivatives are largely composed of carbon, which is considered biologically inert and even biocompatible. Unlike many traditional electronic materials that are toxic (e.g., heavy metal oxides), graphene offers the prospect of direct interfacing between neuromorphic chips and biological systems (such as brain tissue) for bio-hybrid neural networks. The BLAST synaptic transistor mentioned above used a Nafion electrolyte and graphene, both of which are biocompatible, raising the possibility of implantable neuromorphic processors for brain-machine interfaces. Graphene's biocompatibility has been vetted by studies showing that large-area graphene, especially when supported on substrates, does not induce adverse cellular responses. This is

a unique advantage for future neuromorphic wetware interfacing, where artificial neural networks might directly connect with living neurons.

Beyond synapses, there are proposals for graphene-based neuronal devices as well. For example, graphene transistors can act as spiking neurons by using capacitive feedback to create integrate-and-fire oscillations. There is also work on graphene-based optoelectronic neuromorphic systems, where graphene's optical absorption and electro-optic modulation are used to emulate neuronal responses in photonic neural networks [18]. The combination of 2D materials like graphene in neuromorphic architectures can offer enhanced conductivity, scalability, and even new functionality (such as direct sensing). Graphene's transparency and flexibility further allow the creation of wearable or implantable neuromorphic circuits that could process sensory information in a distributed manner.

Challenges in Graphene Neuromorphics. While graphene-based neuromorphic devices are progressing, several challenges remain before they can be deployed at scale. One major issue is device variability. Memristive and analog devices inherently suffer from cycle-to-cycle and device-to-device variability in switching behavior. Graphene can help mitigate some issues (for instance, graphene electrodes can reduce random filament formation sites due to a more uniform electric field), but variability is not eliminated. Controlling the precise movement of ions or defects at the atomic scale is difficult, leading to stochastic behavior. For neuromorphic computing, some variability can be tolerated or even leveraged for stochastic learning, but excessive unpredictability can hurt network performance. Achieving uniform large-area graphene and graphene oxide films is another challenge–any wrinkles or grain boundaries in a graphene electrode could lead to non-uniform switching in an array.

Another challenge is integration with CMOS. Neuromorphic systems may still require CMOS peripheral circuits (for readout, programming, etc.), so graphene devices must be integrated in a way that's compatible with standard processes. For example, graphene synaptic devices might be placed in the back-end (above the silicon layer) as part of a 3D stack. This requires low-temperature processing and careful planarization so as not to disturb the CMOS layers. The good news is that many graphene neuromorphic devices can operate at low voltages (a few volts or less) and do not dissipate much power individually (attowatt-scale switching energy in the BLAST example), which bodes well for large arrays. However, managing heat and power in a dense neuromorphic accelerator with millions or billions of devices will require attention–even tiny leakage currents can sum up.

Despite these challenges, the progress in graphene neuromorphic devices is encouraging. They uniquely combine electronic and ionic behavior (in electrolyte-gated structures), allowing them to mimic the analog dynamics of biological synapses efficiently. They are also well-suited for flexible and biocompatible implementations of neuromorphic systems, opening paths to wearable AI or direct brain-interface computing. In the post-Moore era, where energy efficiency and parallelism are paramount, graphene-based synapses and neurons could become key building blocks for hardware neural networks that operate faster and with far less energy than today's CMOS-based AI accelerators. The coming years will likely see scaled-up demonstrations of graphene neuromorphic chips and further improvements in device reliability, multi-level storage capability (for higher precision weights), and interface electronics.

4. Graphene in Quantum Devices

Quantum computing and quantum information devices represent another frontier of electronics where traditional semiconductor technologies face new challenges. Graphene, with its unusual quantum properties and ability to interact with a variety of other materials, has begun to play a role in several types of quantum devices [19–22]. A comparison of the performance of some typical graphene-based quantum devices can be found in Table 3. In the post-Moore landscape, graphene could contribute both to quantum computing hardware and to quantum classical hybrids (e.g., quantum sensors or interfaces) that augment classical processors. Here we examine graphene's applications in superconducting qubits, spin-based quantum devices, and other emerging quantum technologies.

Table 3. Performance comparison of graphene-based quantum devices.

Device Type	Quantum Effect	Coherence Time/Stability	Control Method
Rhombohedral-stacked multilayer graphene [20]	Quantum anomalous Hall effect	Electric/magnetic field multistability, stable ferromagnetic hysteresis	Vertical electric field, carrier density
Graphene-hBN moiré superlattice [21]	Fractional quantum anomalous Hall effect	Low temperature (near 0 K), narrow plateau width (~10^{10} cm^{-2})	Gate voltage, twist angle
Graphene SQUID [22]	Superconducting quantum interference	Near absolute zero (2 K), reversible superconducting switching	Gate-tuned insulator-superconductor transition

Graphene in Superconducting Qubits. Superconducting qubits (such as the transmon qubit) are among the leading implementations of quantum bits in today's quantum computers. These qubits typically consist of superconducting circuits with Josephson junctions as the non-linear element. A Josephson junction (JJ) is formed by two superconductors separated by a thin barrier through which Cooper pairs tunnel. Interestingly, graphene can serve as the weak-link in a Josephson junction–essentially acting as an atomic-thickness barrier between superconducting electrodes [23,24]. Graphene-based Josephson junctions have been studied since the late 2000s, demonstrating that supercurrents can flow through graphene over micron distances, especially when graphene is encapsulated with hBN to preserve high mobility (Figure 4a). One advantage of using graphene in a JJ is that the junction's properties become tunable by a gate voltage. By applying a gate to a graphene JJ, one can modulate the carrier density in graphene and thereby tune the critical current and junction conductance. This has given rise to the concept of the "gatemon", a gate-tunable superconducting qubit. In gatemon qubits demonstrated with semiconducting nanowires, the Josephson coupling can be adjusted with a gate, offering new flexibility for qubit control. Graphene gatemons have been proposed and explored in experiments [25]: the Josephson junction energy (E_J) can be controlled by the graphene's carrier density, as the carrier density affects the Fermi level, thereby causing changes in the critical current of the Josephson junction. And Josephson junction energy can set the transmon frequency because $f_t = \sqrt{8E_J E_C}/h$, where E_C is the charging energy and h is the Planck constant [26]. While a fully high-coherence graphene-based transmon is still an active research topic, preliminary devices have shown coherent microwave oscillations and serve as qubit prototypes. The superconducting proximity effect in graphene is robust–graphene JJs can support supercurrents up to tens of microamps and have gate-tunable switching currents, effectively acting as superconducting switches.

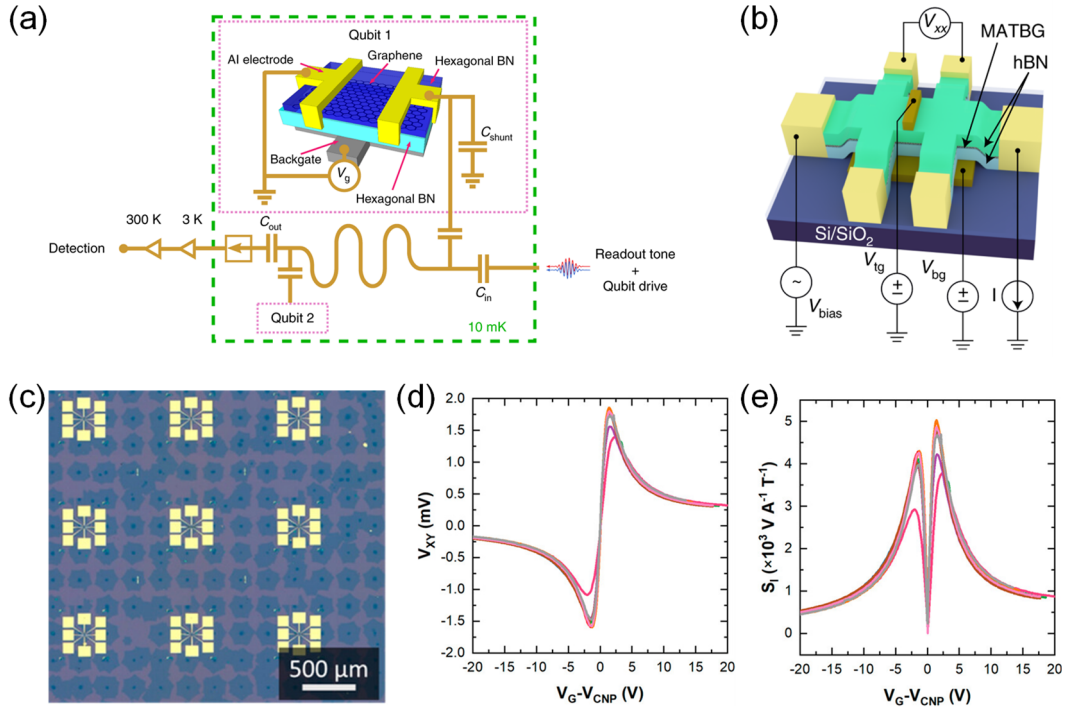

Figure 4. Graphene in quantum devices. (**a**) Schematic illustration of the superconductor–graphene–superconductor junctions encapsulated in hBN and embedded in a circuit quantum electrodynamics platform [23]. (**b**) Schematic illustration of a narrow top gate controlling the underlying region's electronic state [27]. (**c**) Optical micrograph showing graphene crystal arrays on Si/SiO_2 substrate after transfer [28]. (**d**) Hall voltage and (**e**) current-related sensitivity versus gate voltage (relative to charge-neutrality point, CNP), measured at $B \approx 0.37$ T [28].

Graphene's atomically thin nature also means it has little to no bulk two-level system defects which often plague conventional tunnel barrier materials (like amorphous oxides) in Josephson junctions. This could, in principle, lead to cleaner electromagnetic environments for qubits and reduce noise. Indeed, studies of noise in graphene JJs have shown low levels of flicker noise and charge noise, making them attractive from a materials perspective. Additionally, graphene's high transparency junctions can enter novel regimes (between tunneling and ballistic transport) that might realize quantum-coherent superconducting devices with new functionalities. For

example, one can create a superconducting quantum interference device (SQUID) entirely on a graphene sheet by patterning two JJ weak links in graphene–such devices have been used to directly measure the current-phase relationship of graphene JJs and to probe quantum interference at the Dirac point.

Quantum Hall and Topological States. Graphene was the material in which the quantum Hall effect was observed at room temperature, and it harbors unique half-integer quantum Hall states due to its Dirac band structure. In the context of quantum computing, the quantum Hall effect of graphene is mostly of interest for metrology (e.g., resistance standards) rather than computing elements. However, graphene's topological states can inspire quantum device concepts. For instance, under a strong magnetic field, graphene's landau levels could potentially host exotic anyon quasiparticles, though this is largely speculative. More concretely, if one couples graphene to superconductors and a strong spin-orbit coupling material, one could engineer a topological superconducting phase supporting Majorana zero modes–candidate building blocks for topologically protected qubits. A recipe for this could involve placing graphene on a substrate like WSe_2 (which imparts spin-orbit coupling to graphene) and contacting it with a superconductor. Though not yet realized, such a graphene-based topological qubit would leverage the pristine lattice (low disorder) and dual electron/hole nature of graphene's spectrum.

Magic-Angle Twisted Bilayer Graphene (MATBG). A major discovery in condensed matter physics was that two layers of graphene, when stacked with a small twist angle (~1.1°, the "magic angle"), exhibit strong electron correlations, including Mott insulating behavior and superconductivity [29]. This magic-angle graphene is essentially a man-made quantum material where one can tune correlation effects with electric fields and strain. While MATBG is still largely a platform for fundamental physics, its emergence has implications for quantum computing. The superconductivity observed in MATBG is unconventional, and intriguingly, MIT researchers noted that it could be a "promising building block for future quantum-computing devices" [30]. The superconducting state in MATBG might be leveraged to create qubits if it can be integrated into circuits (for example, as a tunable superconducting element). Moreover, the flat bands in MATBG give rise to localized Cooper pairs with a low superfluid stiffness, which has been proposed as a route to achieving high intrinsic phase coherence useful for quantum devices. Although using magic-angle graphene in an actual quantum computer is still speculative, the mere fact that graphene can host superconductivity–and a highly tunable one at that–expands the toolkit for designing novel quantum circuits. Already, researchers have managed to fabricate Josephson junctions where the weak link is a piece of MATBG (Figure 4b) [27], thereby marrying the physics of magic-angle superconductivity with device functionality.

Beyond superconductivity, MATBG and other graphene moiré structures can host interesting quantum states (like quantum anomalous Hall states [20,31] or heavy fermion-like behavior [32,33]) that could be used in quantum simulators. A quantum simulator is a device that emulates complex quantum physics (such as frustrated magnetism or Hubbard model physics) in a controllable way. Graphene's moiré superlattices provide a lattice to trap and manipulate electrons in ways difficult to achieve in real materials, so one could envision a graphene-based analog quantum simulator for certain problems in materials science or even optimization.

Spin Qubits in Graphene. Another approach to quantum computing uses the spin of single electrons confined in quantum dots as qubits (much like in silicon quantum dot qubits). Graphene presents a compelling host for spin qubits because, in its pure form, it has zero nuclear spin (C-12 has no nuclear spin, and natural carbon has ~98.9% C-12). This means a graphene quantum dot would have a spin environment nearly free of hyperfine interaction, a major source of decoherence in other platforms (like GaAs quantum dots). In addition, graphene's weak spin-orbit coupling suggests very long spin coherence times might be possible. The hurdle, again, is the lack of a bandgap–a single layer of graphene cannot confine an electron with electrostatic gates because it never fully blocks conduction. Researchers overcame this by using bilayer graphene, which can be given a tunable bandgap with a perpendicular electric field. In recent experiments, electrostatically defined quantum dots in gapped bilayer graphene have been demonstrated, and a single electron's spin can be isolated. Coupling two such dots to create a two-qubit system for graphene spin qubits is being explored. If successful, graphene spin qubits could leverage long coherence and fast gate-tunability (since graphene electrons move fast) [34]. Coherent control of a graphene spin qubit was reported in a few pioneering studies, but coherence times are not yet on par with silicon spin qubits due to residual disorder and the difficulty of forming well-controlled gaps.

Graphene Quantum Sensors and Interfaces. Beyond computing, graphene can aid in quantum sensing–detecting minute signals at the quantum limit. Its high mobility and low noise make it an excellent detector of electric charges (used in single-electron transistors for charge sensing) and magnetic fields (graphene Hall sensors, Figure 4c–e). Graphene-based Josephson junctions have also been integrated into microwave circuits as parametric amplifiers, which are critical for reading out superconducting qubits. A recent theory even described a graphene JJ parametric amplifier that could operate with high gain and low noise by biasing at certain points [35].

Additionally, graphene's broad optical absorption spectrum and fast carrier dynamics have been exploited in single-photon detectors, which are useful in quantum communication systems for detecting quantum signals. Graphene can absorb a single photon and turn it into an electrical signal (with the help of a bolometric or photovoltaic effect), covering wavelengths from visible to telecom and beyond.

Graphene is carving out multiple roles in quantum technologies. It serves as a versatile quantum-ready material that can interface with superconductors, insulators, and semiconductors, often bringing tunability or superior material qualities (like low noise, high purity) to the system. The fundamental science of graphene in quantum devices is still being actively studied–from understanding how superconductivity arises in twisted layers, to how disorder in graphene affects qubit coherence, to how to induce topological phases. The engineering challenges are significant: for instance, incorporating graphene into a complex qubit chip must account for cryogenic compatibility, nanofabrication of delicate 2D layers, and reproducibility (every qubit should behave the same, which is nontrivial when qubit behavior depends on nanometer-scale details in a graphene flake). Encouragingly, the research community has started to surmount some of these challenges, as evidenced by working graphene JJs in actual superconducting quantum processors and the rapid progress in fabricating high-quality twisted bilayer devices.

Challenges in Graphene Quantum Devices. Despite graphene's compelling quantum properties and promising demonstrations, significant challenges must be overcome before its full potential in quantum technologies can be realized. First and foremost, graphene's extreme sensitivity to atomic-scale details presents a major barrier. Variations in substrate interactions, edge defects, or minute twist-angle deviations (±0.1° in magic-angle graphene) cause unpredictable fluctuations in device performance, making it exceptionally difficult to fabricate identical, high-performance qubits across a chip. This variability affects everything from critical currents in superconducting gatemons to coherence times in spin qubits.

Beyond material imperfections, unresolved questions about graphene's quantum behavior directly impact device capabilities. While graphene itself has low intrinsic noise, parasitic coupling to defects in surrounding materials still limits coherence in superconducting qubits. For spin qubits, charge noise and disorder suppress coherence below theoretical predictions. Crucially, the mechanisms behind key phenomena like unconventional superconductivity in twisted layers or the engineering of viable topological states remain poorly understood, hindering predictive device design.

Finally, translating isolated graphene devices into scalable quantum systems faces substantial integration hurdles. Maintaining the precise conditions required for magic-angle superconductivity or topological phases across large areas and integrating delicate 2D heterostructures with complex multi-qubit circuits—while ensuring cryogenic stability and minimizing gate crosstalk—demands fabrication and engineering solutions far beyond current capabilities.

5. Outlook: Opportunities and Challenges

Looking back, graphene has played an important role in transistors, neuromorphic computing, and quantum technology. Figure 5 shows year-wise milestones of graphene in transistors, neuromorphic computing, and quantum technologies. Looking ahead, the post-Moore era will not be defined by a single winner technology, but rather a convergence of multiple innovations. Graphene is poised to be an important piece of this future computing landscape, not by displacing silicon entirely, but by complementing and enhancing it in areas where silicon struggles (Table 4). For transistors and logic, graphene could extend high-frequency analog and RF performance into regimes silicon cannot reach, and could be integrated vertically to add computing layers in 3D chips. For neuromorphic systems, graphene devices promise orders-of-magnitude improvements in energy efficiency for AI hardware, possibly enabling real-time learning machines that operate at biological levels of power consumption. And in quantum technology, graphene provides a versatile platform to explore and realize new qubit modalities and quantum sensors that might interface seamlessly with classical electronics.

The fundamental challenges are non-trivial. Materials science remains at the forefront: producing wafer-scale graphene with the pristine quality of exfoliated flakes is an ongoing pursuit. Techniques like chemical vapor deposition (CVD) have improved, with methods to reduce grain boundaries and impurities (e.g., single-crystal graphene growth on copper or transition metals). Transferring or directly growing graphene on CMOS-compatible substrates at low temperatures is being refined. Alongside material growth is the need for interface engineering: graphene almost never acts alone in devices–it is part of a stack (dielectrics, electrolytes, contacts, *etc*.). Ensuring clean, controllable interfaces (for example, a uniform 1-nm oxide for gating, or a well-behaved solid electrolyte for ion gating) is essential for device consistency. Fortunately, the toolkit of van der Waals heterostructures–assembling 2D materials like hBN, MoS_2, WSe_2 together with graphene–offers atomic-level control in lab

prototypes. Translating that to manufacturing remains challenging but progress in 2D material integration indicates that industry is seriously evaluating these options.

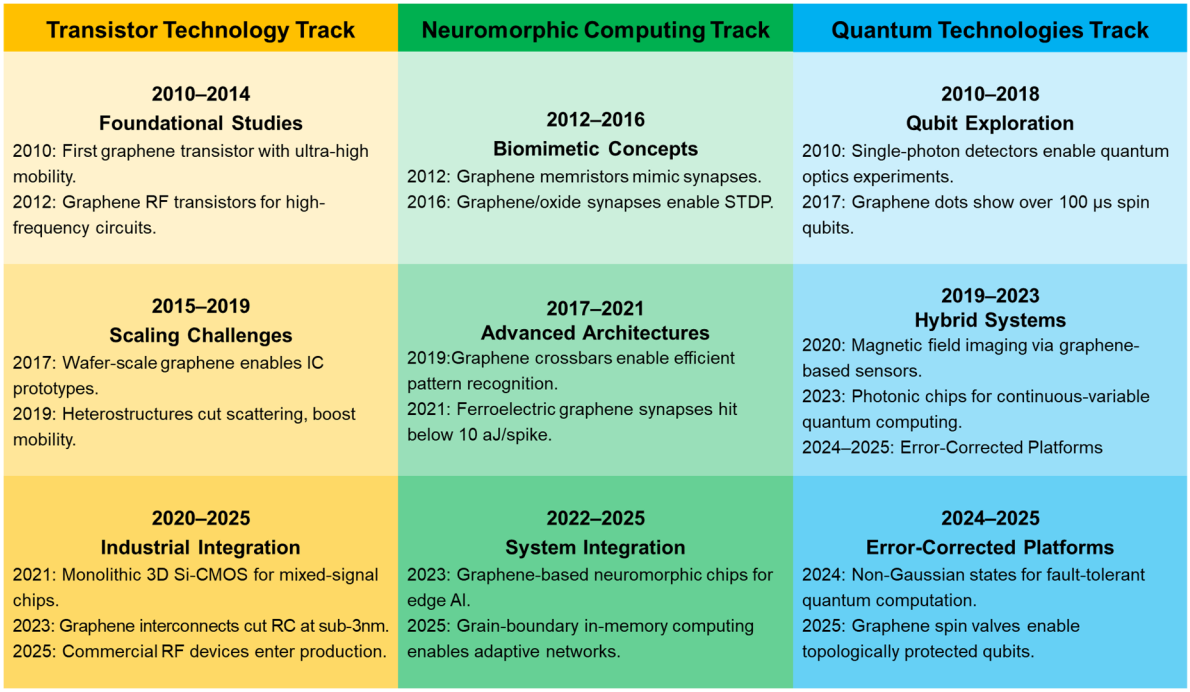

Figure 5. Year-wise milestones of graphene in transistors, neuromorphic computing, and quantum technologies.

Table 4. Graphene's roles in post-Moore computing paradigms and key challenges.

Applications	Main Role of Graphene	Key Challenges
Transistors	/ High-mobility channel for ultra-scaled transistors and RF devices / Terahertz operation / Integration into 3D architectures	/ Absence of a bandgap / Solutions: graphene nanoribbons, bilayer graphene with induced gap, novel designs (e.g., tunnel FETs, barristors) / Low-resistance contacts / Large-area synthesis of high-quality graphene
Neuromorphic computing	/ Synaptic elements / Brain-like learning in memristors and synaptic transistors / Operation with extremely low energy dissipation	/ Device variability / Retention of analog states / Large-scale integration of millions of devices / CMOS compatibility / Managing sneak-path currents in crossbar arrays
Quantum devices	/ Tunable medium in superconducting qubits (e.g., graphene Josephson junctions) / Host for long-coherence quantum states (e.g., spin, topological modes)	/ Maintaining quantum coherence by minimizing defects, charge noise, and magnetic impurities / Reproducible fabrication of graphene quantum dots and moiré structures devices

Another overarching challenge is circuit architecture. Using graphene devices effectively might require re-thinking circuit designs. For instance, logic circuits built from graphene barristors or tunneling devices may need new logic families or error correction schemes to deal with lower voltage swings. Neuromorphic architectures will have to embrace analog computing principles, co-designing device dynamics with learning algorithms that can tolerate device non-idealities. The co-development of algorithms and hardware is especially pertinent in neuromorphic and quantum domains–graphene devices might open certain capabilities (e.g., online learning with

metaplastic synapses, or fast voltage-tunable qubit gates) that algorithms can exploit. Conversely, knowing the algorithms' tolerance for variability or noise can relax device requirements.

In the big picture, graphene's journey from isolated flakes in physics labs to a cornerstone of post-Moore electronics is still underway. It has been over 15 years since its discovery, and while we haven't replaced silicon transistors with graphene, we now better appreciate *where* graphene excels: in roles that complement silicon, adding new functionality (like optical modulation, sensing, or memristive behavior) or pushing performance beyond silicon's limits (in speed, flexibility, or miniaturization). The coming era of "More-than-Moore" heterogenous integration may see a single system where silicon logic, memory, RF communications, and sensor interfaces are all integrated–potentially with graphene and other 2D materials bridging the gaps between them.

Graphene's compatibility with CMOS (being carbon-based, it introduces no new incompatible dopants or deep levels in silicon) is a major advantage in integration. We might soon see niche applications where graphene is inserted into commercial products–for example, a graphene RF amplifier chip for 6G wireless, or a graphene-based neural network accelerator for edge AI. Success in these early applications could pave the way for broader adoption.

In conclusion, graphene stands out as a multifaceted material that addresses key challenges of the post-Moore computing landscape: it offers a path to faster transistors when scaling hits a wall, a means to hardware AI that breaks the von Neumann bottleneck, and a playground for integrating quantum physics into practical devices. The fundamental science of graphene–its Dirac fermions, its strong carbon bonds, its surface-only existence–makes it simultaneously exciting and demanding to work with. The engineering required–from mastering atomic-layer growth to designing novel circuit architectures–is driving innovation across disciplines. As research and development continue, graphene is likely to transition from a laboratory curiosity to an essential ingredient in the evolution of computing, helping to carry the baton of progress in a world beyond the traditional limits of Moore's Law.

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